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ANN Based Control and Estimation of Direct Torque Controlled Induction Motor Drive

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Abstract – Direct Torque Control (DTC) of Induction Motor drive has quick torque response without complex orientation transformation and inner loop current control. Although DTC has some drawbacks, such as the torque and flux ripple. The control scheme performance relies on the accurate selection of the switching voltage vector. This paper proposed simple structured neural network based new identification method for flux position estimation, sector selection and stator voltage vector selection for induction motors using direct torque control (DTC) method. The ANN based speed controller has been introduced to achieve good dynamic performance of induction motor drive. The Levenberg-Marquardt back-propagation technique has been used to train the neural network. Proposed simple structured network facilitates a short training and processing times. The stator flux is estimated by using the modified integration with amplitude limiter algorithms to overcome drawbacks of pure integrator. The conventional flux position estimator, sector selector and stator voltage vector selector based modified direct torque control (MDTC) scheme compared with the proposed scheme and the results are validated through both by simulation and experimentation.

Keywords – ANN based speed controller, direct torque control (DTC), flux position estimator

I. INTRODUCTION

The induction motor is very popular in variable speed drives due to its well known advantages of simple construction, ruggedness, and inexpensive and available at all power ratings. Progress in the field of power electronics and microelectronics enables the application of induction motors for high-performance drives where traditionally only DC motors were applied. Thanks to sophisticate control methods, induction motor drives offer the same control capabilities as high performance four quadrant DC drives. A major revolution in the area of induction motor control was invention of field-oriented control (FOC) or vector control by Blaschke [1] and Hasse [2].

In vector control methods, it is necessary to determine correctly the orientation of the rotor flux vector, lack of which leads to poor response of the drive. The main drawback of FOC scheme is the complexity. The new technique was developed to find out different solutions for the induction motor torque control, reducing the complexity of FOC schemes known as Direct Torque control (DTC).

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Direct Torque control (DTC) for induction motor was introduced about twenty years ago by Japanese and German researchers Takahashi and Noguchi [3]-[4]. DTC was considered as an alternative to the field oriented control scheme to overcome the weakness of scheme.

In DTC, the torque and flux are directly controlled by using the selection of optimum voltage vectors. The switching logic control facilitate the generation of the stator voltage space vector, with a suitable choice of the switching pattern of the inverter, on the basis of the knowledge of the sector (supplied by the stator flux model block) in which the stator flux lies, and of the amplitudes of the stator flux and the torque. The sector identification depends on the accurate estimation of stator flux position. Novel artificial-intelligence-based stator flux estimator for induction motor has been proposed by [5].

The ANNs are capable of learning the desired mapping between the inputs and outputs signals of the system without knowing the exact mathematical model of the system. Since the ANNs do not use the mathematical model of the system, the same. The ANNs are excellent estimators in non linear systems [6] - [8]. Various ANN based control strategies have been developed for direct torque control induction motor drive to overcome the scheme drawback [9] - [11].

In this paper, neural network flux position estimation, sector selection and switching vector selection scheme proposed, and ANN based speed controller used to reduce the current ripple by regulating the switching frequency, are proposed. Total harmonic distortion (THD) of the stator current analysis has been also presented in this work.

The organization of this paper goes on in the following order. In Section II, it will be presented the Mathematical model and basic concept of DTC for induction motor drive. In Section III and IV it will be described flux estimation algorithm and artificial neural networks and implementation of ANN to the DTC scheme. The simulation and experimental results will be presented in Section V and VI for the proposed scheme validation. In Sections VII, it will be presented the conclusions of this work.

II. MATHEMATICAL MODEL OF INDUCTION MOTOR AND BASIC CONCEPT OF DTC

The dynamic model of the induction motor is derived by transforming the three phase quantities into two phase direct and quadrature axes quantities. The mathematical model in compact form can be given in the stationary reference frame as follows [12].

$$\begin{pmatrix} v_{ds} \\ v_{qs} \\ v_{dr} \\ v_{qr} \end{pmatrix} = \begin{pmatrix} R_s+L_s p & 0 & L_m p & 0 \\ 0 & R_s+L_s p & 0 & L_m p \\ L_m p & \omega_r L_m & R_r+L_r p & \omega_r L_r \\ -\omega_r L_m & L_m p & -\omega_r L & R_r+L_r p \end{pmatrix} \times \begin{pmatrix} i_{ds} \\ i_{qs} \\ i_{dr} \\ i_{qr} \end{pmatrix} \quad (1)$$

$$\psi_{ds} = L_s i_{ds} + L_r i_{dr} \ , \ \Psi_{qs} = L_s i_{qs} + L_r i_{qr} \quad (2)$$

$$\psi_{dr} = L_r i_{dr} + L_s i_{ds} \ , \ \Psi_{qr} = L_r i_{qr} + L_s i_{qs} \quad (3)$$

where v_{ds}, v_{qs}, i_{ds}, i_{qs} R_s, L_s, R_r, L_r, L_m, Ψ_{ds}, Ψ_{qs}, Ψ_{dr}, Ψ_{qr} and θ_r are the d-q axes voltages and currents, stator resistance, stator inductance, rotor resistance, rotor inductance, mutual inductance between the stator and rotor windings, stator flux linkages, rotor flux linkages and the rotor position respectively.

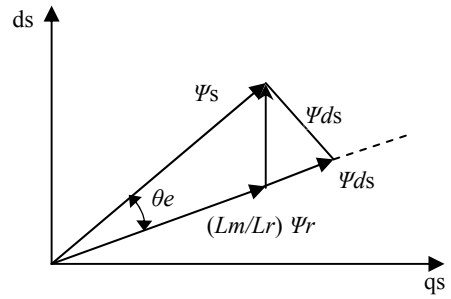


Fig. 1: Stator and rotor flux-linkage space vectors.

The electromagnetic torque obtained from machine flux linkages and currents is as:

$$T_e = \frac{3}{2}\frac{P}{2} L_m (i_{qs}\psi_{dr} - i_{ds}\psi_{qr}) \quad (4)$$

where T_e, P, Ψ_{dr}, Ψ_{qr} are the electromagnetic torque, number of poles, rotor d-q axes fluxes respectively.

The electromagnetic torque equation can also be obtained in stationary reference frame as:

$$T_e = \frac{3}{2}\frac{P}{2}\frac{L_m}{\sigma L_r L_s}|\psi_r||\psi_s|\sin\theta_e \quad (5)$$

where σ = Leakage coefficient$=1-\left(\frac{L_m^{\,2}}{L_s L_r}\right)$

The angle between the stator and rotor flux linkage space vectors is θ_e *as* shown in Fig. 1.

The stator flux linkage, voltage and torque equations in d-q axis stationary reference frame can be obtained as follows

$$v_{ds} = R_s i_{ds} + p\psi_{ds} \quad (6)$$

$$v_{qs} = R_s i_{qs} + p\psi_{qs} \quad (7)$$

$$\psi_{ds} = \int (v_{ds} - R_s i_{ds})dt \quad (8)$$

$$\psi_{qs} = \int (v_{qs} - R_s i_{qs})dt \quad (9)$$

$$\psi_s = \sqrt{\psi_{ds}^{\,2} + \psi_{qs}^{\,2}} \quad (10)$$

$$\theta_e = \tan^{-1}\left(\frac{\psi_{qs}}{\psi_{ds}}\right) \quad (11)$$

From equation (5) it is clear that the motor torque can be varied by changing the rotor or stator flux vectors. The rotor time constant of a standard squirrel-cage induction machine is very large, thus the rotor flux linkage changes slowly compared to the stator flux linkage. However, during a short transient, the rotor flux is almost unchanged. Thus rapid changes of the electromagnetic torque can be produced by rotating the stator flux in the required direction, which is determined by the torque command. On the other hand the stator flux can instantaneously be accelerated or decelerated by applying proper stator voltage phasors. Depending on the position of the stator flux, it is possible to switch on the suitable voltage vectors to control both flux and torque.

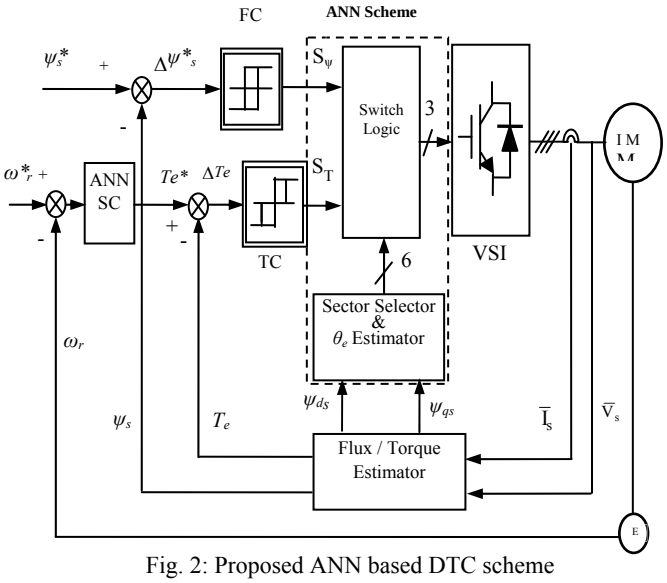


Fig. 2: Proposed ANN based DTC scheme

The switching logic given below in the table 1 is developed from the output signals of hysteresis comparators; represent the increment (decrement) of the flux (torque).

Table 1: Switching logic

Conditions for Flux	S_Ψ
$\|\Psi_s\| \leq \|\Psi_s^*\| - \|\Delta\Psi_s\|$	1
$\|\Psi_s\| \geq \|\Psi_s^*\| + \|\Delta\Psi_s\|$	0
Conditions for Torque	S_T
$\|T_e\| \leq \|T_e^*\| - \|\Delta T_e\|$	1
$\|T_e\| = \|T_e^*\|$	0
$\|T_e\| \geq \|T_e^*\| + \|\Delta T_e\|$	-1

The first sector of -30° to 30° in conventional , is taken as 0° to 60° and the new modified optimal switching voltage vector table is given in table 2**,** where k (i.e. k = 1, 2..., 6) indicates the sector position of stator flux.

Table 2: Voltage switching vector table (MDTC)

	$\|\Psi s\|\uparrow$ ($\Delta\Psi s$ =1)	$\|\Psi s\|\downarrow$ ($\Delta\Psi s$ =0)
$T_e\uparrow$ (ΔT_e =1)	v_{k+1}	v_{k-2}
$T_e\uparrow$ (ΔT_e = 0)	v_7 or v_8	v_7 or v_8
$T_e\downarrow$ (ΔT_e = -1)	v_{k+5}	v_{k+4}

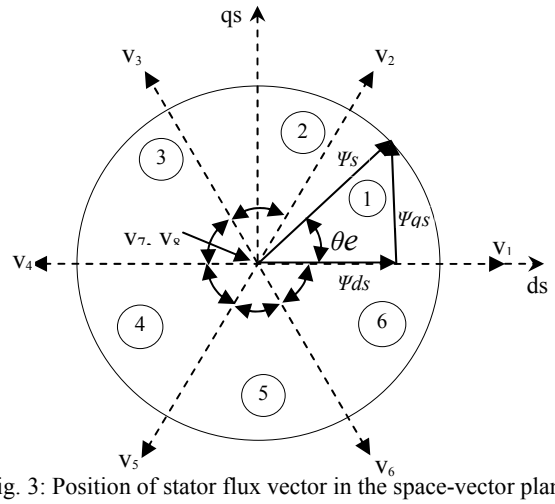


Fig. 3: Position of stator flux vector in the space-vector plane (MDTC).

III. Stator Flux Estimator Algorithm

In (8) and (9), pure integrators are applied to estimate the stator flux. Notably, initial value error and dc-offset problems exist herein. To improve these problems, solution proposed to use the low-pass filter that has the input–output relation given by a newly proposed integration algorithm is used [13], the Simulink model is developed for stator flux estimation algorithm as shown in Fig. 4.

The input output relation of the low pass filter is given by

$$y = \frac{1}{s + \omega_c}.x \qquad (12)$$

By choosing a low value of cut off frequency ω_c leads to a better integration, but higher dc bias. A higher value of cutoff frequency ω_c changes the integration output. The d-q axis stator fluxes in the stationary reference frame are mainly computed by the integration of back emf in the d-q frame which can be obtained by the abc to d-q transformation. The stator flux amplitude and angle are calculated from (10) and (11), the absolute value of flux is dc bias signal obtained from the flux limiter block output. These signals are transferred into original form by using the Polar to Cartesian. This algorithm is suitable for the constant flux operation.

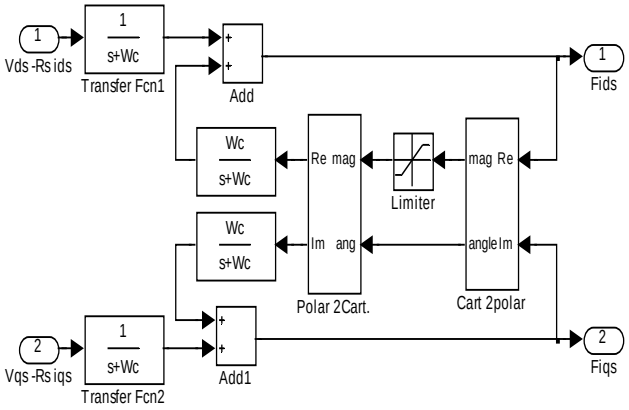


Fig. 4: Simulink model of integration method for stator flux estimation.

IV. Artificial Neural Network Based Estimator and Controller

ANN has a very significant role in the field of artificial intelligence. The artificial neurons learn from the data fed to them and keep on decreasing the error during training time and once trained properly, their results are very much same to the results required from them, thus referred to as universal approximators [14]. The most popular neural network used by researchers are the multilayer feed forward neural network trained by the back propagation algorithm [15] .There are different kinds of neural networks classified according to operations they perform or the way of interconnection of neurons. Some approaches use neural networks for parameters estimation of electrical machines in feedback control of their speeds [16, 17].

A. ANN based voltage vector estimator

Here we have used a feed forward neural network to select the voltage vector. For this purpose different configurations of networks were used and the best configured network is proposed and this scheme is depicted in the Fig. 2. The relation of variables used in the proposed scheme is as shown in Fig. 3.There are three neural networks. First is to estimate the value of stator flux position, θ_e as shown in the Fig. 5. This is the angle between the stator flux and the rotor flux. It is a two input-one output feed-forward network with three layers. The input layer has 6 neurons of hyperbolic tangent sigmoid transfer function, first hidden layer has 4 neurons of log sigmoid transfer function and the output layer has 1 neuron of linear function. The necessary steps to adjust these weights associated with the hidden neurons can be made through the training of the neurons. Levenberg-Marquardt back-propagation method is used here for training the network [18]. The inputs given are'd-axis stator flux' and 'q-axis stator flux'.

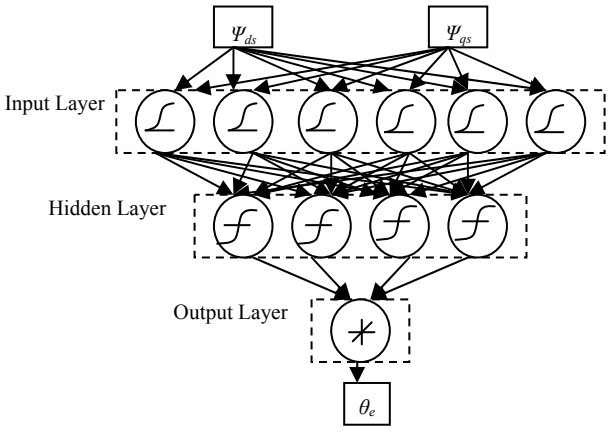


Fig. 5: Feed forward ANN for theta estimation.

Second neural network is used to determine the sector number for the estimated value of θ_e. There are total of six sectors, each sector of 60 degree. Again three layers of neurons are used but with a 5-4-1 feed forward configuration as shown in Fig. 6. Input layer is of log sigmoid transfer function, hidden layer is of hyperbolic

tangent sigmoid function and the output layer is of linear transfer function. The training method used was Levenberg-Marquardt back-propagation. The input given is the angle theta since sector selection is purely based on theta.

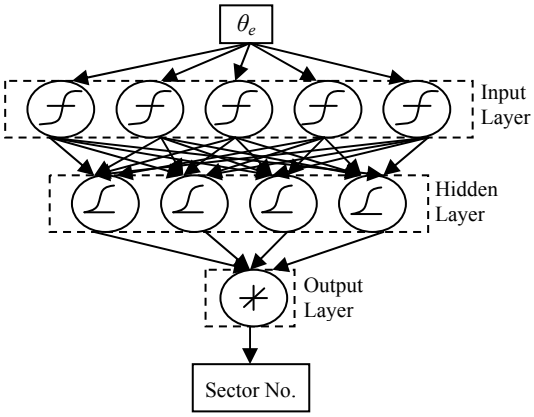


Fig. 6: Feed forward ANN for sector selection

Last neural network is for the selection of voltage vector as given in Fig. 7, which is based on three inputs, flux, torque and the sector. Network taken this time is a 3-5-1 feed forward network with first layer of log sigmoid transfer function, second layer of hyperbolic tangent sigmoid transfer function and third layer of linear transfer function. Training method used was again Levenberg-Marquardt back-propagation. All the three neural networks were trained to performance 0.00001 mse. Here mse is a network performance function and it measures the network's performance according to the mean of squared errors (mse).

The back-propagation algorithm is used to train the neural networks. The training function used is Levenberg-Marquardt back-propagation, it updates weights and bias values according to Levenberg-Marquardt optimization.

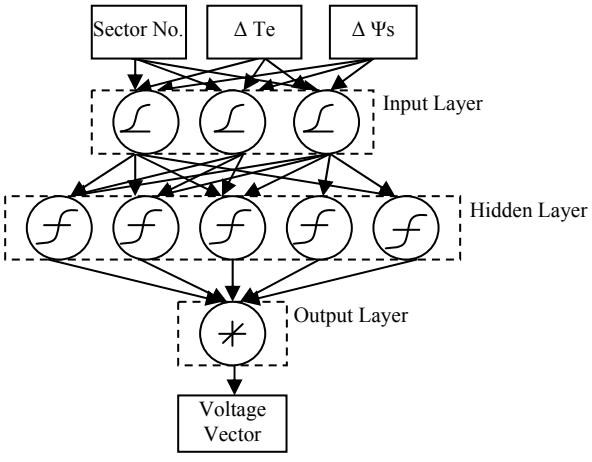


Fig. 7: Feed forward ANN for sector selection

As soon as the training procedure is over, the neural network gives almost the same output pattern for the same or nearby values of input. This tendency of the neural networks which approximates the output for new input data is the reason for which they are used as intelligent systems.

B. ANN Speed Controller

The input and output of the ANN controller can be obtained from the PI controller input output and which can be written as:

$$Y(s) = X(s)\left(K_p + \frac{K_i}{s}\right) \tag{13}$$

Where X(s) is the input and Y(s) is the output of PI controller, K_p and K_i are the proportional and integral gain constants.

The equation (13) can be written in the difference form as:

$$y(n)y(n-1) + K_p\left[x(n) - X(n-1) + K_i x(n)\right] \tag{14}$$

Where n is present time constant and (n-1) is previous time constant. The equation for speed controller can be obtained as:

$$x(n) = \omega_{ref}(n) - \omega_r(n) \tag{15}$$

y(n) is the output of speed controller which is the controlling torque for the present control scheme of induction motor drive. The ANN based speed controller (ANNSC) structure is as shown in Fig. 8.

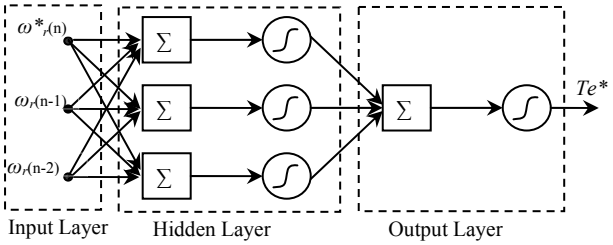


Fig. 8: Feed forward ANN speed controller

V. SIMULATION RESULTS

The results of simulation obtained in this work are for the induction motor of 3 HP and parameters as given in appendix. The machine model is implemented for modified DTC scheme and proposed ANN based DTC scheme using Matlab /Simulink.

First the MDTC scheme is applied to the induction motor to check the performance under no load and then switch to full load (12-Nm) condition at 0.4 sec. The speed reversal has been applied at 0.55 sec and the results of stator currents for all conditions are presented in Fig. 9 (a). Fig. 9 (c) and Fig. 9 (e) shows the torque and the speed response under steady state and transient condition for conventional DTC scheme. Fig. 9 (b) and Fig. 9 (d) shows the results of the stator current and torque, (zoomed for comparison) which present more ripples.

The results for ANN based DTC scheme under the same loading conditions, speed reversal as in case of MDTC scheme are presented in Fig. 10 (a) and Fig. 10 (e). The torque ripples and stator current harmonic content are reduced as seen in the results. Fig. 10 (b) and Fig. 10 (d) shows that the ripples in the stator current and torque is comparatively less which supports accuracy in the ANN based estimator and validation for ANN based DTC scheme. Fig. 10 (f) shows the smoothness in the flux plot of the proposed scheme as compared to its counterpart of MDTC scheme as in Fig. 9 (f). For comparison purposes, the harmonic current analysis is performed at spectra frequency of 1000 Hz and the fundamental current

frequency of 50 Hz. The harmonic analysis is carried for Fig. 9 (a) and Fig. 10 (a) under no load (0.1 sec to 0.3 sec period) and load (0.4 sec to 0.5 sec period) condition and results are shown in Fig. 11 and Fig. 12. Comparative harmonic analysis results during no-load and load operation have been depicted in Table 3.

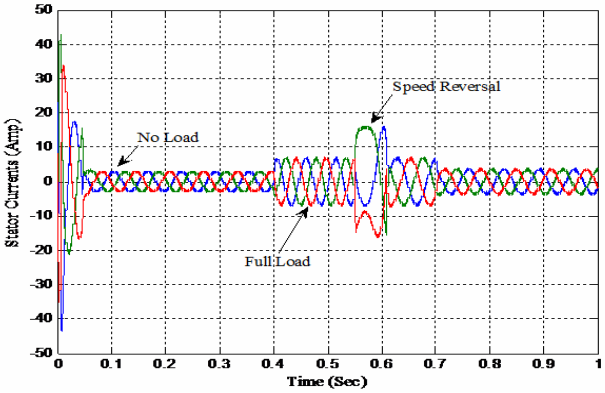


Fig. 9 (a): Stator current response of MDTC scheme for all operating conditions.

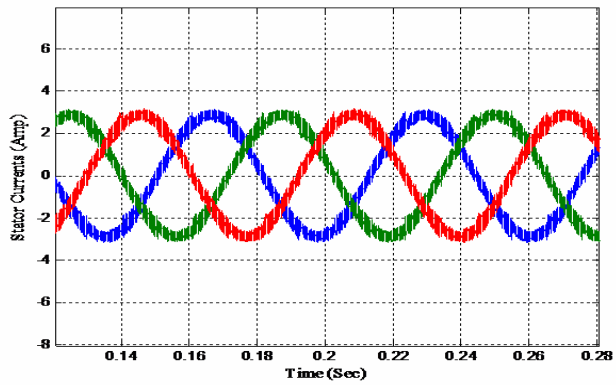


Fig. 9 (b): Stator current (Zoomed) response of MDTC scheme for no load condition

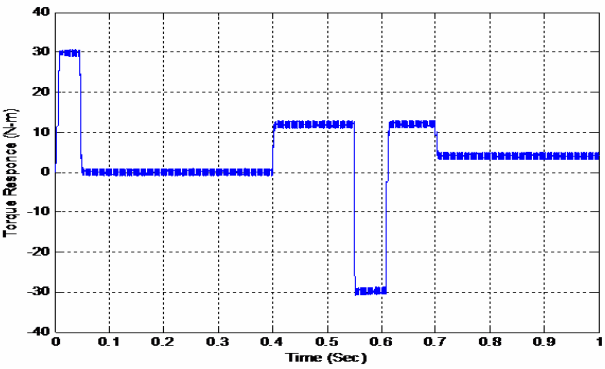


Fig. 9 (c): Torque response of MDTC scheme for all conditions.

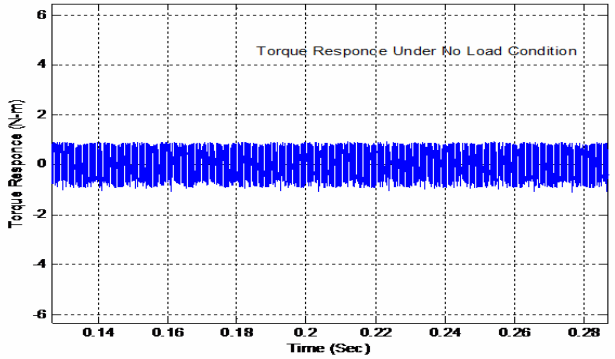


Fig. 9 (d): Zoomed torque response for time interval 0.14 sec to 0.28 sec of Fig.9 (c).

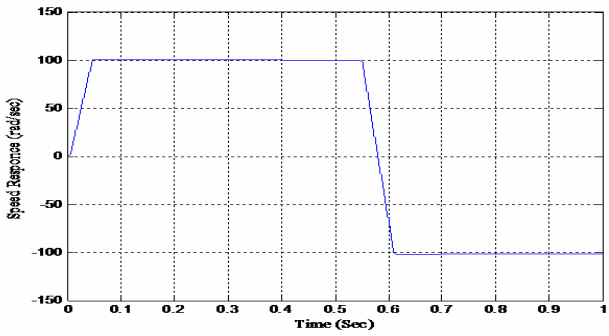


Fig. 9 (e): Speed response of conventional DTC scheme

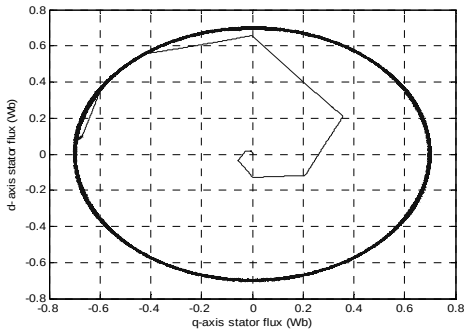


Fig. 9 (f): d-q-axis stator flux plot (MDTC Scheme).

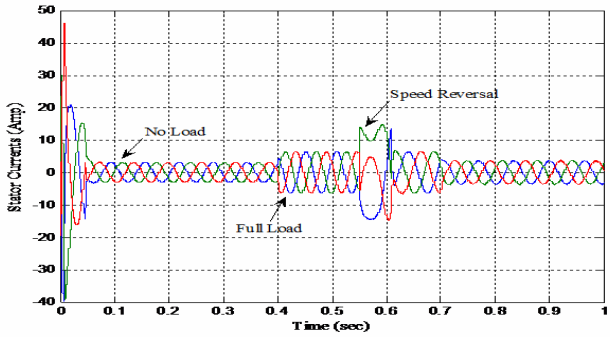


Fig. 10 (a): Stator current response of ANN based DTC scheme for all operating conditions.

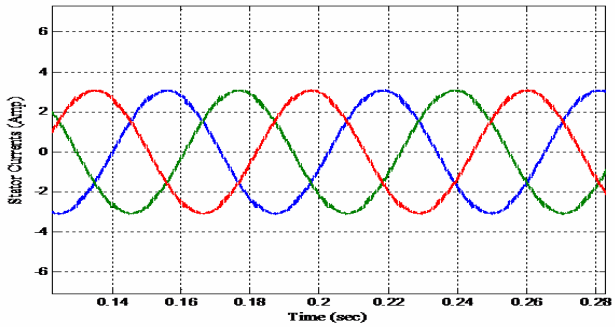


Fig. 10 (b): Stator current (Zoomed) response of ANN based DTC scheme for no load condition

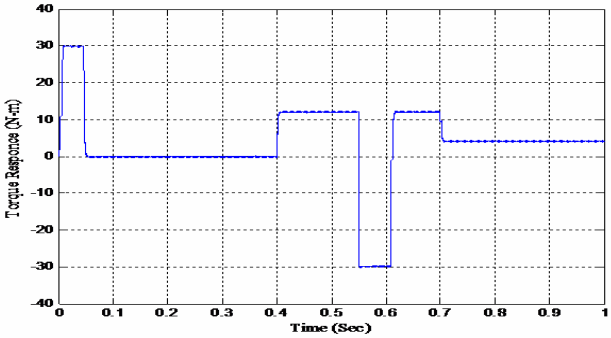


Fig. 10 (c): Torque response of ANN based DTC scheme for all conditions

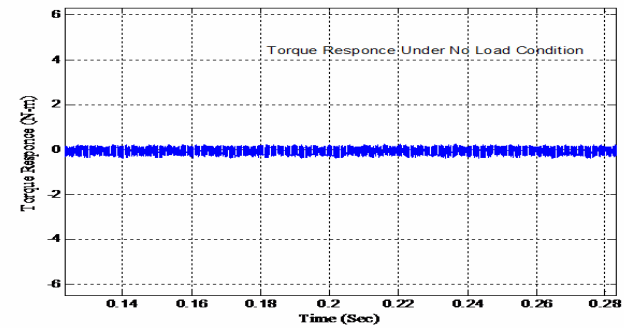


Fig.10 (d): Zoomed torque response for time interval 0.14 sec to 0.28 sec of Fig. 10 (c).

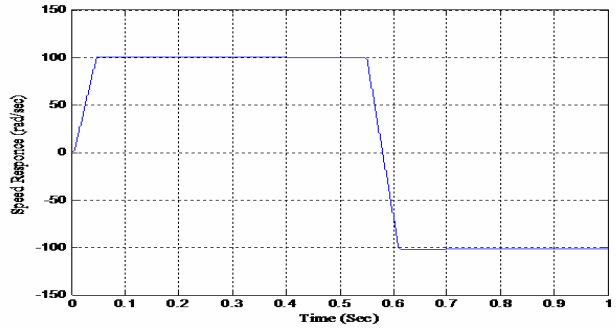


Fig. 10(e): Speed response of ANN based DTC scheme

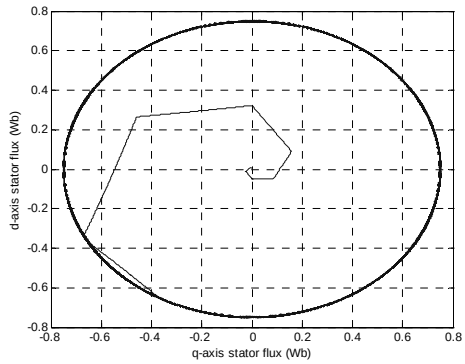
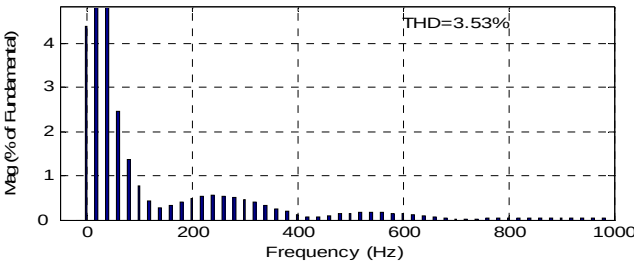
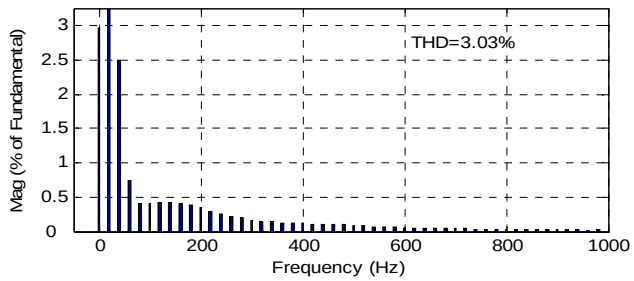


Fig. 10 (f): d-q-axis stator flux plot (ANN based DTC scheme)

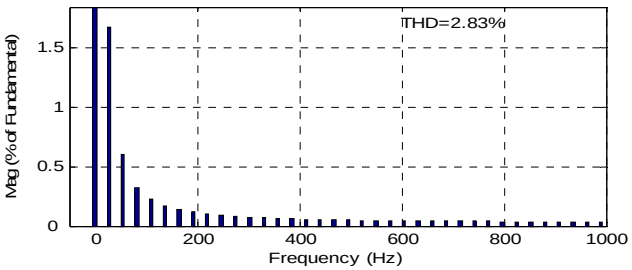


(a)

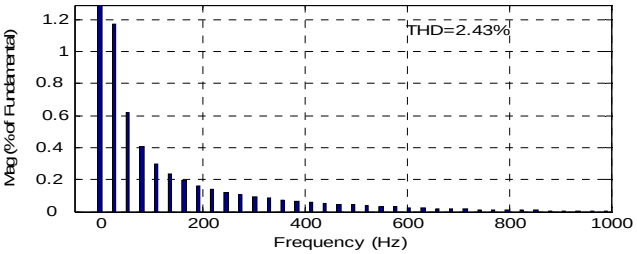


(b)

Fig. 11: Harmonic spectrum of stator current under no load (a) and load (b) condition for MDTC



(a)



(b)

Fig. 12: Harmonic spectrum of stator current under no load (a) and load (b) condition for ANN based DTC

Table 3: Comparison of total harmonic distortion for the modified DTC and ANN based DTC schemes

Control Scheme	THD (%) of Stator current (Amp)	
	No load	load
Modified DTC	3.53%	3.03%
ANN based DTC	2.83%	2.43%

VI. Experimental Results

In order to make the experimental validation of the effectiveness of the proposed DTC scheme for torque ripple reduction, a DSP-based induction motor drive system has been built. The experimental setup includes a fully digital controlled IGBT 5kVA Semikron make inverter and a 2.2-kW, 415-V, 50-Hz, four-pole induction motor. The control scheme has been implemented on dSPACE controller board DS-1104 which consist a DSP processor MPC8240 of 250 MHz. The dSPACE has 4 multiplexed channel, 16-bit sample and hold ADC, 4 parallel channels, 12-bit sample and hold ADC and 8 channel of digital to analog converter (DAC), with 16-bit resolution. The induction motor has the same parameters applied in simulation. The machine currents i_a and i_b sensed by LEM LA 55-P current sensor and voltage sensor LEM LV 100-1000V used to sense the dc bus voltage these signals were interfaced into the controller through an analog to digital converter (A/D) which is separate peripheral unit of controller board. The photo of experimental set is shown in Fig. 13. The controller sampling time set to 0.0001 sec and DSP board was controlled with a PC.

Fig. 14 (b) shows the corresponding waveform for the of d-q axis stator fluxes reflect the reduction in ripples and confirms the effectiveness of flux ripple reduction to decrease the torque ripple as depicted in Fig. 16 (b) .

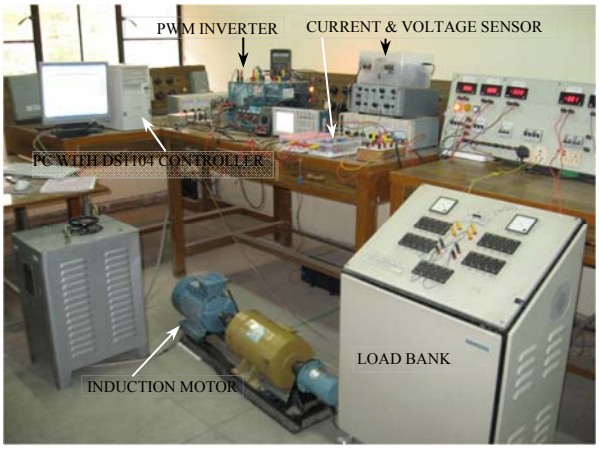


Fig. 13: Photo of experimental setup

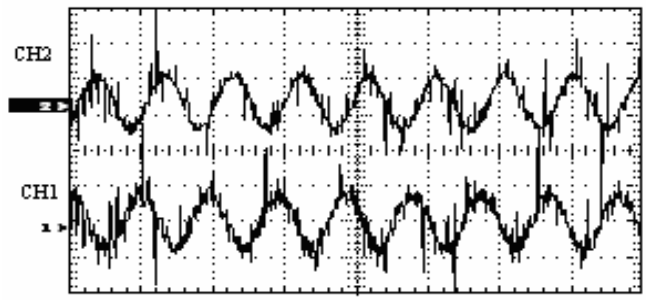


Fig. 14 (a)

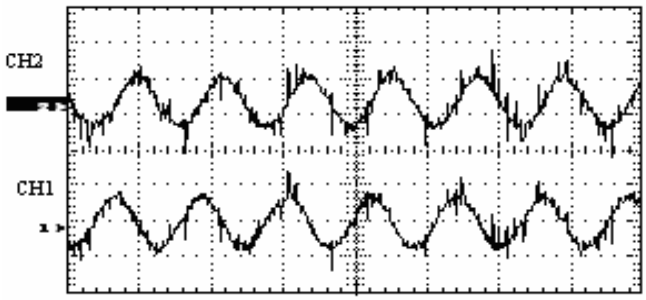


Fig. 14 (b)

Experimental response of the d axis stator flux (upper trace) and q axis stator flux (lower trace) (a) for MDTC. (b) ANN based DTC (in y axis flux 1 Wb/div, in x axis 50 ms/div)

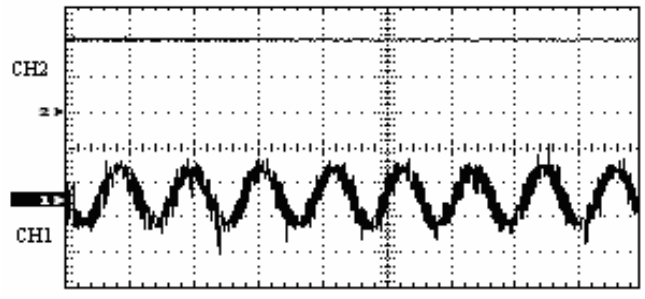


Fig. 15 (a)

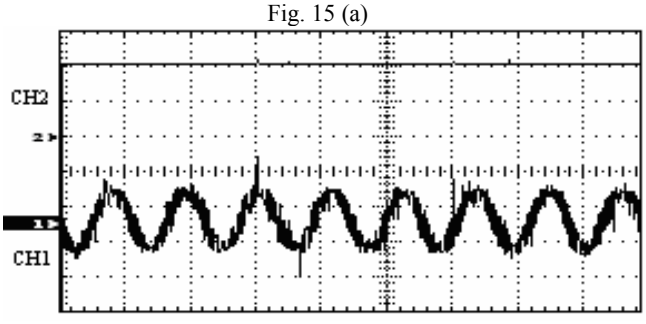


Fig. 15(b)

Experimental response of the rotor speed (upper trace) & stator current i_a (lower trace) (a) for MDTC. (b) ANN based DTC i_a = 3A/div rotor speed =50 (rad/sec)/div, 50 ms/div

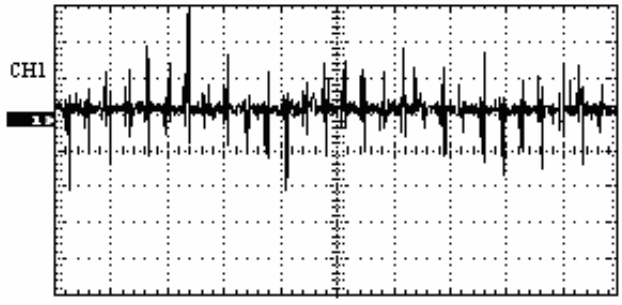


Fig. 16 (a)

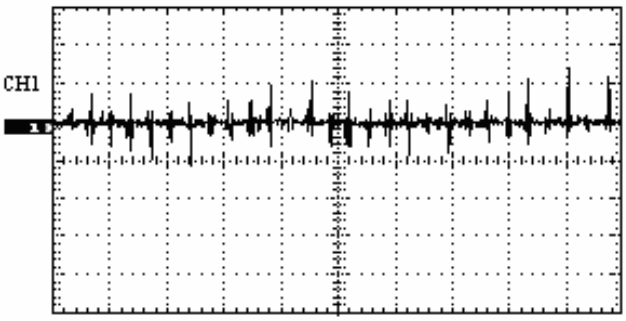


Fig. 16(b)

Experimental response of torque (a) MDTC. (b) ANN based DTC under steady state (0.5-Nm./div), 50 ms/div

VII. Conclusion

In this paper a new ANN based speed controller, flux position estimation, sector selection and the switching voltage vector selection has been proposed for direct torque controlled induction motor drive. The proposed scheme performance is compared with the modified DTC scheme under the steady state and dynamic conditions. According to the simulation and experimental results of a (3HP) test motor, amplitude of the stator flux ripple and developed torque ripple are reduced by notable amount with good speed dynamic. The both results support that the ANN based DTC scheme has better performance than modified DTC scheme. The feasibility and validity of the proposed identification have been proved by the excellent experimental results.

Appendix

The parameters of the three-phase Induction Motor, employed for simulation purpose, in SI units are

2.2 kW (3HP) Three phase 415V, 50 Hz, 1415 rpm,
R_s = 1.95 Ω, R_r =1.66 Ω, L_{ls} = 244mH, L_{lr}= 243mH,
L_m = 369mH, P = 4, J = 0.025 kg/m^2, B = 1e-5 Nms

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Performance Evaluation of Three Single Phase Voltage Source Inverter Based Configuration of DSTATCOM

Alka Adya[1] Bhim Singh[2] A.P. Mittal[3]

Abstract – This paper deals with the detailed modeling and simulation of a three-phase four-wire Distribution Static Compensator (DSTATCOM) used as a shunt compensator. This DSTATCOM configuration consists of three single-phase voltage source inverter (VSI) bridges having a common dc link. The model is developed using MATLAB/ Simulink and tested for a variety of linear as well as non-linear loads. The ability of this compensator is demonstrated in improving various facets of power quality viz. power factor correction, voltage regulation and harmonic reduction. Comparisons with existing and well known DSTATCOM configurations are made and analyzed in detail.

Keywords – DSTATCOM, power quality, voltage regulation, harmonic reduction

I. INTRODUCTION

There has been a rapid rise in the development of power electronic based compensators. This has led to the development of FACTS as well as custom power devices for transmission as well as distribution systems [1-3]. Power quality issues have been a major concern for power engineers worldwide [4-8]. As a result, development of custom power devices is increasing for load compensation in distribution systems [9-13]. DSTATCOM is a popular shunt compensator having the ability to provide reactive power compensation. Both three-phase and single-phase DSTATCOMs can be designed for compensation of different load configuration. One of the most commonly used configurations of DSTATCOM is the three-leg VSI based configuration for three-phase, three-wire system. A three-phase, four-wire system also has an additional conductor. In the presence of neutral conductor, possible DSTATCOM configurations are four-leg VSI or a three-single phase VSI. This paper deals with the modeling and simulation of a three-single phase VSIs based DSTATCOM which has a number of advantages over its four-leg VSI counterpart. Each single–phase VSI has lower kVA rating and the cost of components such as DC capacitor, Insulated Gate Bipolar Transistor (IGBT) switches having low voltage and the current rating can also be effectively reduced. Moreover, modular approach involving three single-phase VSIs gives better flexibility and enhanced control.

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II. STYLE INFORMATION

The DSTATCOM system configuration considered here consists of a three-phase, four-wire ac source feeding a variety of loads. A three-phase, four-wire ac source with supply impedance (L_s, R_s) feeds power to balanced/unbalanced linear/non-linear loads. Fig. 1 shows the basic diagram of DSTATCOM connected as shunt compensator to the distribution system via three single phase transformers. The DSTATCOM configuration considered here consists of three independent single-phase voltage source inverters having a common dc bus. Three-VSI bridges are connected together at the dc link at which a dc bus capacitor (C_{dc}) provides a self-supporting dc bus. This scheme requires three single-phase transformers or a three-phase transformer with access to individual windings. The control scheme consists of providing gating pulses to the three VSI bridges. The control algorithm is suitably modified to improve various power quality features. Another advantage of this DSTATCOM configuration is that the current in neutral wire is controlled to zero value.

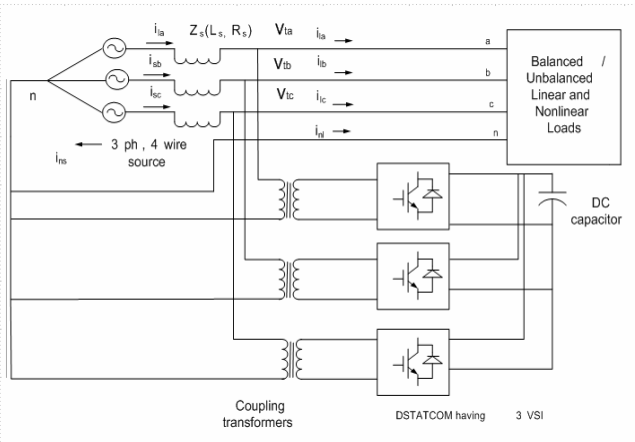


Fig. 1: Schematic diagram of DSTATCOM (3 VSI configuration) connected to a three-phase, four-wire distribution system.

III. PROBLEMS ASSOCIATED WITH NEUTRAL CURRENT

In three-phase, four-wire system, the current in the neutral conductor is the sum of three line currents. If the system is perfectly balanced, the neutral current is zero. However, practical distribution system is never perfectly balanced and the neutral current mitigation always becomes an important issue for power system engineers [7, 11-13]. The main cause of neutral conductor current is load unbalancing and presence of non-linear loads. Moreover, under certain conditions, even perfectly balanced single-phase loads could result in significant neutral currents. The presence of non-linear loads having non-sinusoidal

current in nature adds up to neutral current magnitude. The triplen current harmonics are in phase with each other for three-phase-circuits and it results in net rise of neutral current. Recent advances in power electronics technology have led to a tremendous increase in loads such as computers, air conditioning equipment, florescent lights with electronic ballasts, office equipment etc. The configuration of DSTATCOM considered in this work is able to reduce neutral current in the neutral conductor to negligible amount even when there is appreciable current in the load neutral conductor due to load unbalancing and harmonics currents.

IV. CONTROL OF DSTATCOM

The most commonly used control techniques involve instantaneous reactive power theory (p-q theory), synchronous reference frame theory, indirect current control theory etc. The current control algorithm employing hysteresis rule based carrier-less PWM current control is effective and simple [12-13]. To realize this, a current controlled voltage source inverter is used as a DSTATCOM. One Proportional Integral (PI) controller is used to regulate the dc link voltage and helps to improve power-factor to unity. Two PI controllers are needed to regulate terminal voltage at PCC. The generation of reference supply currents involves computation of two components as:

A. Computation of In-Phase Components of Reference Supply Currents

The amplitude of in-phase component of reference supply currents (I_{spdr}) is computed using PI controller over the average value of dc bus voltage of the DSTATCOM (v_{dc}) and reference dc voltage (v_{dcr}) as:

$$I_{spdr(n)} = I_{spdr(n-1)} + K_{pd}\{v_{de(n)} - v_{de(n-1)}\} + K_{id}\, v_{de(n)} \quad (1)$$

where $v_{de(n)} = v_{dcr} - v_{dca(n)}$ denotes the error in v_{dc} calculated over reference v_{dcr} and average value of v_{dc} at the n^{th} sampling instant. K_{pd} and K_{id} are proportional and integral gains of the dc bus voltage PI controller. The in-phase components of the reference supply currents (i_{sadr}, i_{sbdr}, i_{scdr}) are computed using the in-phase unit current templates (u_a, u_b, u_c) derived from the filtered ac terminal voltages at PCC (v_{ta}, v_{tb}, v_{tc}) as:

$$u_a = v_{ta}/V_{tm} \quad (2)$$

$$u_b = v_{tb}/V_t \quad (3)$$

$$u_c = v_{tc}/V_{tm} \quad (4)$$

where V_{tm} is amplitude of the supply voltage and it is computed as:

$$V_{tm} = \{2/3(v_{ta}^2 + v_{tb}^2 + v_{tc}^2)\}^{1/2} \quad (5)$$

The computation of in-phase components of reference supply currents is carried out as:

$$i_{sadr} = I_{spdr}\, u_a \quad (6)$$

$$i_{sbdr} = I_{spdr}\, u_b \quad (7)$$

$$i_{scdr} = I_{spdr}\, u_c \quad (8)$$

B. Computation of Quadrature Components of Reference Supply Currents

The amplitude of quadrature component of reference supply currents (I_{spqr}) is computed using another PI controller over the amplitude of supply voltage (V_{tm}) and its reference (V_{tmr}).

$$I_{spqr(n)} = I_{spqr(n-1)} + K_{pq}\{v_{ae(n)} - v_{ae(n-1)}\} + K_{iq}\, v_{ae(n)} \quad (9)$$

where $v_{ae(n)} = V_{tmr} - V_{tm(n)}$ denotes the error calculated over reference V_{tmr} and V_{tm} estimated using eq(5) and K_{pq} and K_{iq} are the proportional and integral gains of the second PI controller. The quadrature unit current templates (w_a, w_b, w_c) are derived from in-phase unit current templates (u_a, u_b, u_c). Three-phase quadrature components of the reference supply currents (i_{saqr}, i_{sbqr}, i_{scqr}) are computed using the output of second PI controller (I_{spqr}) and quadrature unit current vectors as:

$$i_{saqr} = I_{spqr}\, w_a \quad (10)$$

$$i_{sbqr} = I_{spqr}\, w \quad (11)$$

$$i_{scqr} = I_{spqr}\, w_c \quad (12)$$

C. Computation of Reference Supply Currents

Three-phase reference supply currents (i_{sar}, i_{sbr}, i_{scr}) are computed by adding in-phase (i_{sadr}, i_{sbdr}, i_{scdr}) and quadrature components of supply currents (i_{saqr}, i_{sbqr}, i_{scqr}) as:

$$i_{sar} = i_{sadr} + i_{saqr} \quad (13)$$

$$i_{sbr} = i_{sbdr} + i_{sbqr} \quad (14)$$

$$i_{scr} = i_{scdr} + i_{scqr} \quad (15)$$

Hysteresis PWM current controller is employed over the reference supply current (i_{sar}, i_{sbr}, i_{scr},) and sensed supply currents (i_{sa}, i_{sb}, i_{sb}) to generate 12 gating pulses for the IGBTs of the single phase VSI bridge. Three such VSI bridges (connected for all the three phases) are suitably controlled using hysteresis current controller. Thus, a total of 12 gating pulses (4 per VSI) are generated simultaneously (Fig. 2).

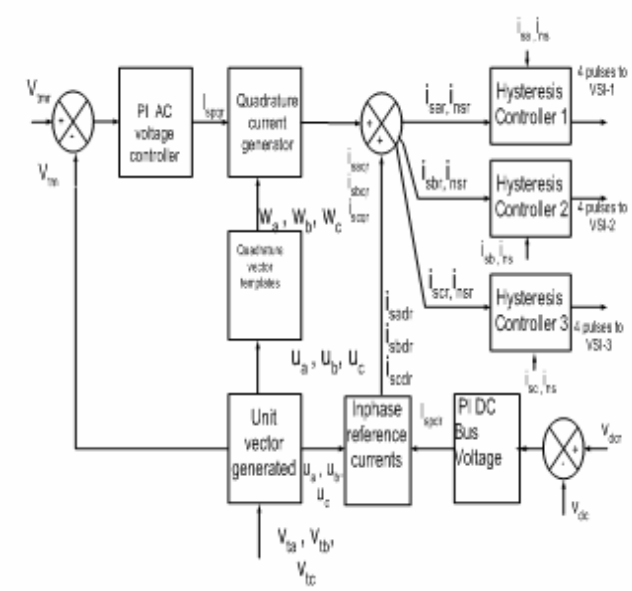


Fig. 2: Control scheme for three-VSI.

V. MATHEMATICAL MODELING OF SYSTEM COMPONENTS

This section discusses the modeling of supply system, DSTATCOM and linear as well as nonlinear loads.

A. Modeling of Three-Phase, Three-Wire AC System with DSTATCOM

The modeling of the supply can be given in terms of three volt-ampere equations as:

$$v_{sa} = i_{sa}R_s + L_s p i_{sa} + n\, v_{ta} \quad (16)$$

$$v_{sb} = i_{sb}R_s + L_s p i_{sb} + n\, v_{tb} \quad (17)$$

$$v_{sc} = i_{sc}R_s + L_s p i_{sc} + n\, v_{tc} \quad (18)$$

where p denotes the time differential operator (d/dt). v_{sa}, v_{sb} and v_{sc} are the three-phase supply voltages. v_{ta}, v_{tb} and v_{tc} are the three-phase voltages at point of common coupling (PCC),n is the turns ratio of the transformer. i_{sa}, i_{sb}, i_{sc} are three-phase supply currents, R_s and L_s are the supply resistance and inductance parameters.

B. Modeling of DSTATCOM

The DSTATCOM configuration with three-single phase VSIs is connected in shunt configuration to the system. Each single phase VSI has two legs and it is connected to each phase and neutral. The dc link of three VSIs is held in common by a single dc bus capacitor as represented in Fig. 3. The control of each VSI is independent. The model equations for three-legged DSTATCOM can be written as:

$$v_{ta} = i_{ca}R_c + L_c p i_{ca} + v_{ca} \quad (19)$$

$$v_{tb} = i_{cb}R_c + L_c p i_{cb} + v_{cb} \quad (20)$$

$$v_{tc} = i_{cc}R_c + L_c p i_{cc} + v_{cc} \quad (21)$$

where v_{ta}, v_{tb} and v_{tc} are the three-phase ac voltages at the PCC, i_{ca}, i_{cb}, i_{cc} are the DSTATCOM currents, R_c and L_c are the DSTATCOM resistance and inductance parameters. The first order differential equation for DC link voltage (v_{dc}) can be written as:

$$p v_{dc} = (i_{cad} + i_{cbd} + i_{ccd}) / C_{dc} \quad (22)$$

where v_{dc} denotes the DC link voltage at the DSTATCOM terminals and SA_1, SA_2, SB_1, SB_2, SC_1, SC_2 are the switching functions decided by switching logic of the three phases of DSTATCOM. The three-phase ac voltages at the terminals of DSTATCOM (v_{ca}, v_{cb} and v_{cc}) are calculated as:

$$v_{ca} = (SA_1 - SA_2)\, v_{dc} \quad (23)$$

$$v_{cb} = (SB_1 - SB_2)\, v_{dc} \quad (24)$$

$$v_{cc} = (SC_1 - SC_2)\, v_{dc} \quad (25)$$

The charging currents i_{cad}, i_{cbd}, i_{ccd} *are expressed as:*

$$i_{cad} = i_{ca}(SA_1 - SA_2) \quad (26)$$

$$i_{cbd} = i_{ca}(SB_1 - SB_2) \quad (27)$$

$$i_{ccd} = i_{ca}(SC_1 - SC_2) \quad (28)$$

C. Modeling of Loads

Different nature of load (linear, nonlinear) are modeled here.

1) Linear Load

Three-phase balanced and unbalanced star connected resistive inductive loads (Z_{la}, Z_{lb}, Z_{lc}) are connected on a three-phase, four-wire system (Fig. 4a) with switches to disconnect any phase of the loads. These inductive–resistive three phase loads may be modeled by the following equations:

$$v_{ta} = R_l\, i_{la} + L_l p i_{la} \quad (29)$$

$$v_{tb} = R_l\, i_{lb} + L_l p i_{lb} \quad (30)$$

$$v_{tc} = R_l\, i_{lc} + L_l p i_{lc} \quad (31)$$

where i_{la}, i_{lb} and i_{lc} are the three-phase load currents, R_l and L_l are the load resistance and inductance parameters.

2) Non-Linear Load

A set of three single-phase nonlinear loads is connected to three-phase, four-wire grid system (Fig. 4b). Each phase load consists of a single-phase uncontrolled bridge rectifier with an AC input impedance and DC link capacitive-resistive (R-C) loading. When the diodes are conducting, AC supply mains is connected to the load. The basic equations for the three phase loads are written as:

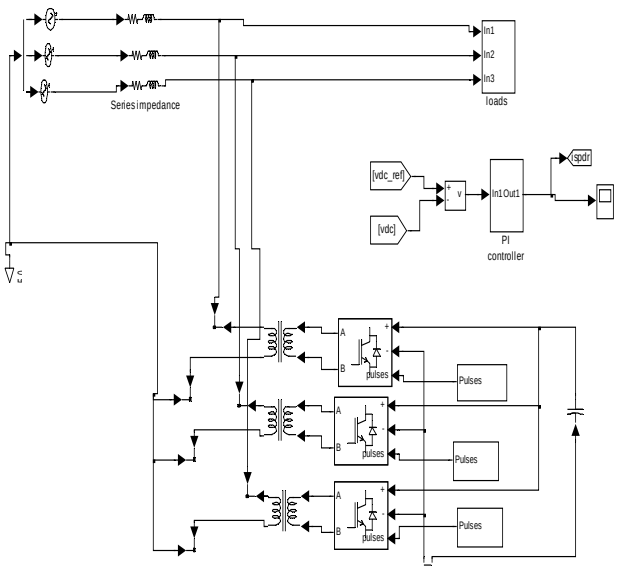


Fig. 3: MATLAB based model for the DSTATCOM configuration.

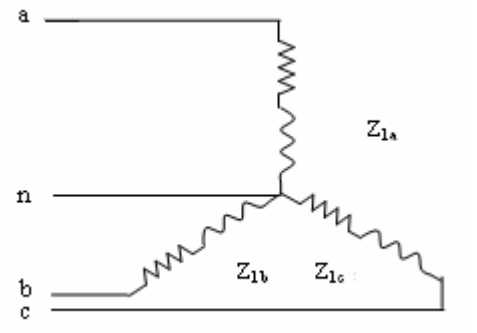


Fig. 4a: Linear load connected in star configuration.

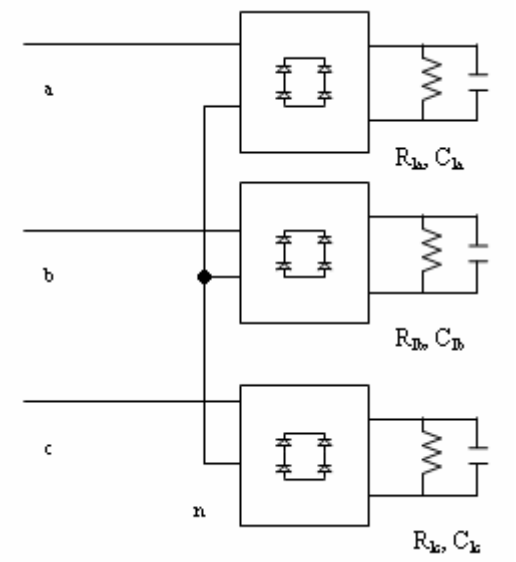


Fig. 4b: Non-Linear load connected for four-wire system.

$$v_{sa} = v_{la} + i_{la}R_s + L_s p i_{la} \quad (32)$$

$$v_{sb} = v_{lb} + i_{lb}R_s + L_s p i_{lb} \quad (33)$$
$$v_{sc} = v_{lc} + i_{lc}R_s + L_s p i_{lc} \quad (34)$$

where v_{sa}, v_{sb}, v_{sc} are three-phase ac voltages, R_s, L_s are supply impedance, v_{la}, v_{lb}, v_{lc} are voltages across load capacitors C_{la}, C_{lb}, C_{lc}. The load capacitor equations can be written as:

$$pv_{la} = (i_{da} - i_{ra}) / C_{la} \quad (35)$$
$$pv_{lb} = (i_{db} - i_{rb}) / C_{lb} \quad (36)$$
$$pv_{lc} = (i_{dc} - i_{rc}) / C_{lc} \quad (37)$$

where currents i_{la}, i_{lb}, i_{lc} are the load currents drawn from ac mains and i_{da}, i_{db}, i_{dc} are their magnitudes. The currents i_{ra}, i_{rb}, i_{rc} are dc load currents (v_{ta}/R_{la}), (v_{tb}/R_{lb}) and (v_{tc}/R_{lc}) respectively. The load neutral current (i_{nl}) can be calculated from three-phase load currents i_{la}, i_{lb}, i_{lc} as:

$$i_{nl} = -(i_{la} + i_{lb} + i_{lc}) \quad (38)$$

VI. Results And Discussion

The developed model for DSTATCOM is tested over a variety of linear and non-linear loads for power quality improvement.

A. Performance of DSTATCOM with Linear Loads

The performance of DSTATCOM with linear loads is considered here for a variety of power quality improvement features viz. power factor correction and voltage regulation.

1) Power factor correction and Load balancing

Fig. 5 shows the performance of DSTATCOM for power-factor correction with R-L lagging load (20.5kW, 0.8pf). A PI controller is realized over the dc bus to regulate the dc link voltage to a value of 550V. The dynamic performance of variables like supply voltage (v_s), supply currents (i_s), load currents (i_l), compensator currents (i_c) and sensed and reference values of dc link voltage (v_{dc}) are shown to demonstrate the performance of DSTATCOM. It is observed that DSTATCOM improves the supply power-factor to unity. The supply currents are balanced, sinusoidal and in-phase with the voltages. For dynamic performance of DSTATCOM, load unbalancing is introduced at t= 0.66sec, one phase of load ('a' phase) is switched off (13.67 kW) and at t=0.76sec, the load is put back to 20.5kW. The control action provides a self-supporting dc bus.

2) Voltage regulation and Load balancing

Fig. 6 shows the response of the DSTATCOM for ac voltage regulation at PCC with 20.5kW, 0.8 lagging power-factor linear (R-L) load. The transient response for the various performance variables are shown for load changing from three-phase (30kW) to two-phase (20kW) at t=0.57sec. The dynamic performance of variables like supply voltage (v_s), terminal voltage at PCC (v_t), supply currents (i_s), load currents (i_l), DSTATCOM currents (i_c), sensed and reference values of dc link voltages (v_{dc}) and sensed and reference values of ac terminal voltage (v_{tm}) is observed in this figure. At t=0.57sec, when one phase (phase 'a') of the load is thrown off, dc link voltage tends to increase. This reflects in the form of an overshoot in DC link voltage. However, by controller action, the dc bus voltage of DSTATCOM and ac terminal voltage at PCC are regulated at their reference values. The supply currents are sinusoidal, balanced and slightly leading with respect to supply voltages. DSTATCOM maintains ac terminal voltage without any abnormal surge. The supply currents are sinusoidal, balanced and reduced in magnitude for transient period after t=0.57sec when the load currents are unbalanced.

B. Performance of DSTATCOM with Non-Linear Loads

Here a balanced three-phase nonlinear load is represented in the form of three single-phase uncontrolled diode bridge rectifiers feeding resistive load with parallel capacitor filter.

(1) Power Factor Correction and Harmonic Reduction

Fig. 7 shows the transient response of the DSTATCOM for power-factor correction and harmonic reduction with nonlinear loads. The response for the various performance variables are shown in this figure for R=25Ω and C=500μF (14.5kW) connected at end of diode rectifier. The load on the system is changed from 14.5kW to 19.8kW at t=0.4sec and back at t=0.6sec. The reference dc link voltage is set to 550V. It is observed that at t=0.4sec, the dc link voltage dips a little but the DSTATCOM regulates V_{dc} to reference value. It is observed that the supply neutral conductor has negligible current even though the load and DSTATCOM neutral conductors carry large currents. The waveform and Total Harmonic Distortion (THD) for supply current and load current are shown in Fig. 8 and Fig. 9. It is observed that THD of load current 63.88% is reduced to 3.88% in supply current.

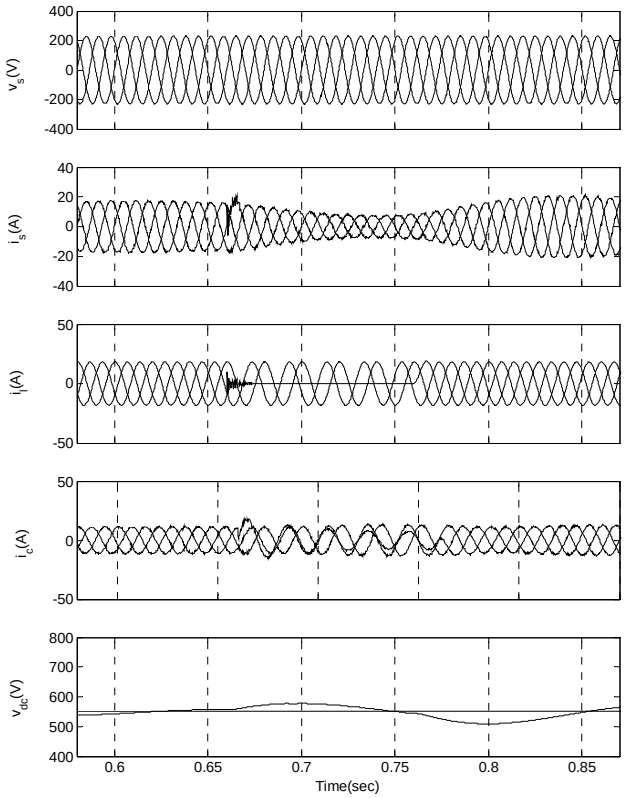


Fig. 5: Performance of DSTATCOM with linear loads for power factor correction

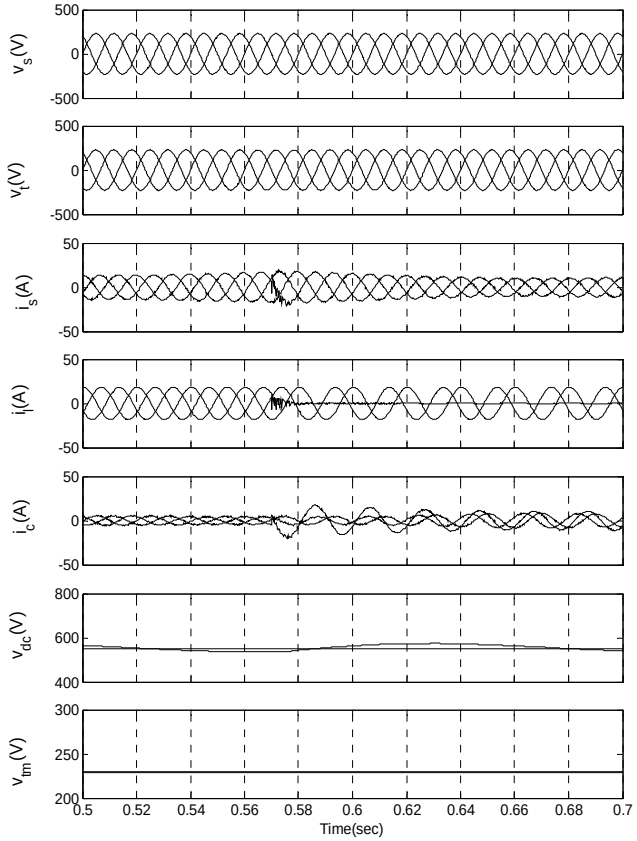


Fig. 6: Performance of DSTATCOM with linear loads for voltage regulation.

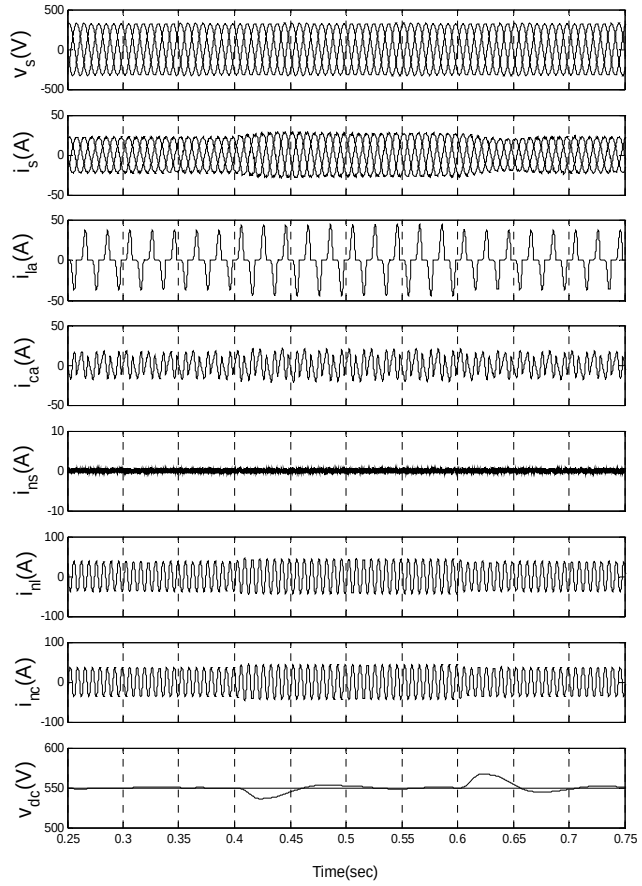
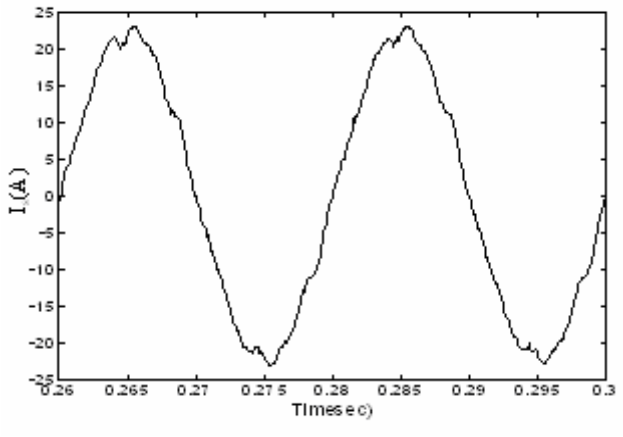


Fig. 7: Performance of DSTATCOM with non-linear load for power factor correction and harmonic reduction.



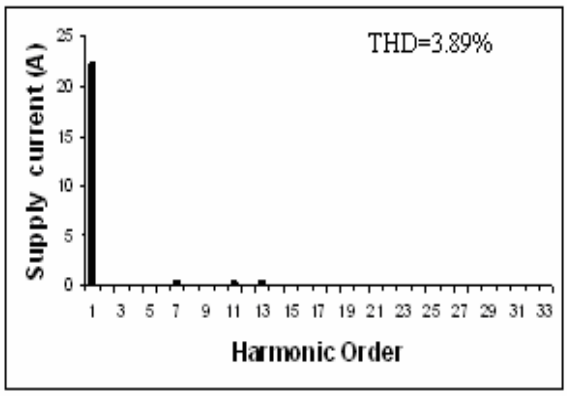
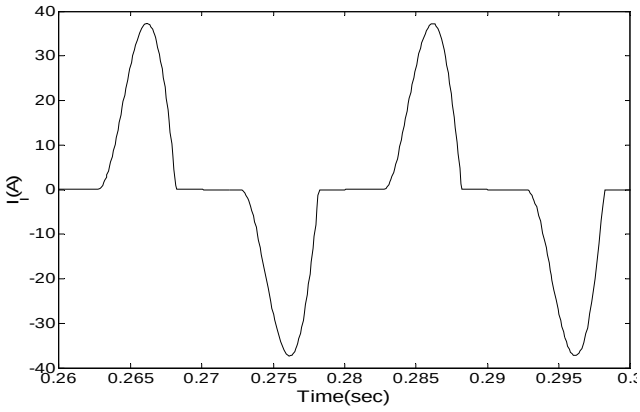


Fig. 8: Waveform and harmonic spectrum for supply current.



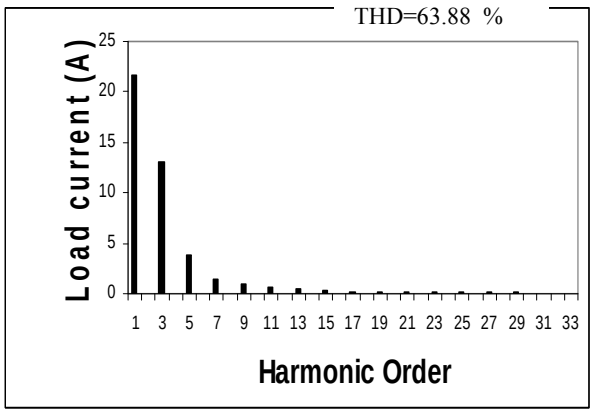


Fig. 9: Waveform and harmonic spectrum for load current I_L

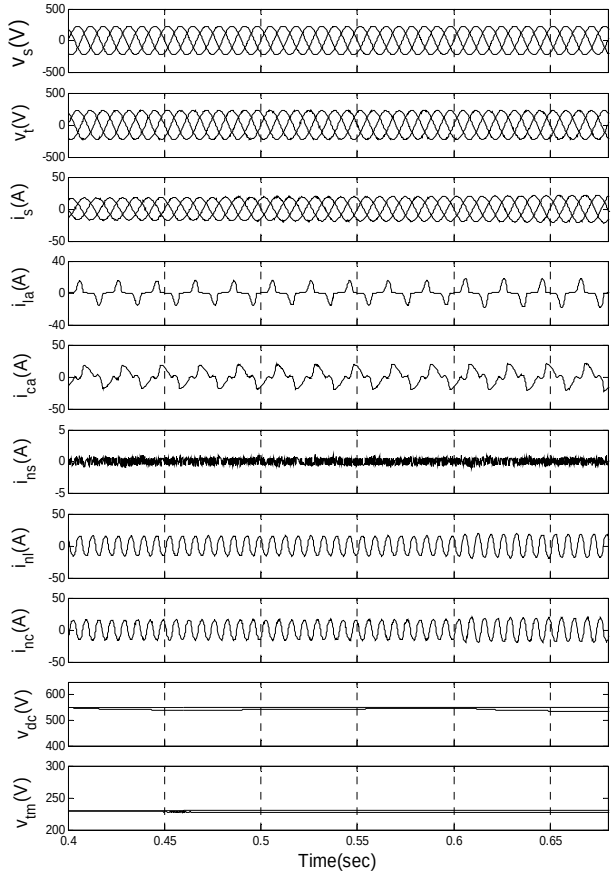


Fig. 10: Performance of DSTATCOM for voltage regulation and harmonic reduction

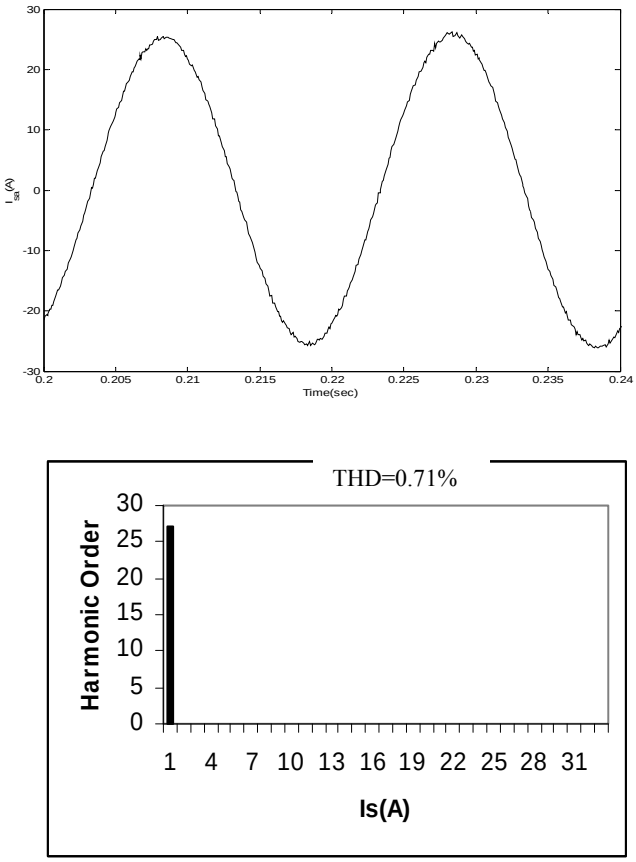


Fig. 11: Waveform and harmonic spectrum for supply current (I_s).

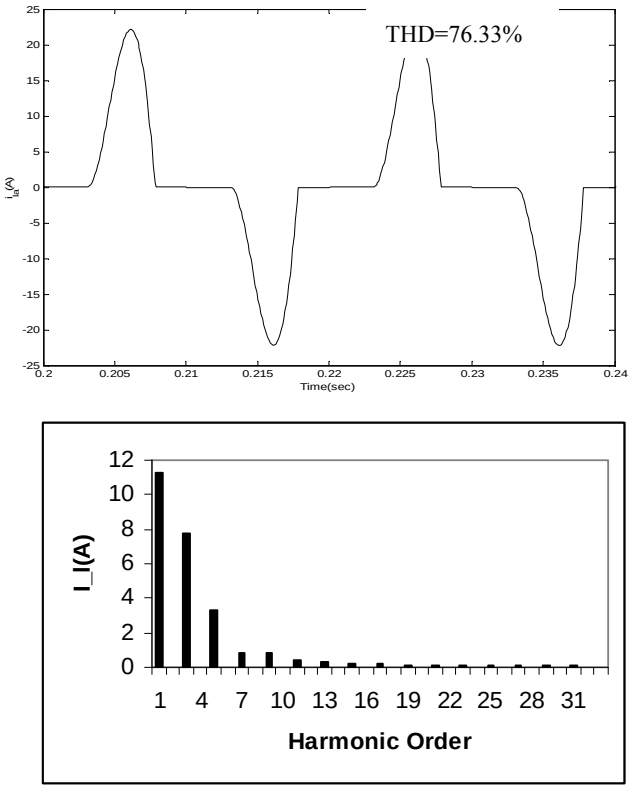


Fig. 12: Waveform and harmonic spectrum for load current (I_l)

(2) Voltage Regulation and Load Balancing

Fig. 10 shows the transient response under non-linear load for voltage regulation and harmonic elimination. Here, two PI controllers are used–one over V_{dc} and the other over V_{tm}. The dynamic response for the various performance variables are shown in this figure for R=50 Ω and C= 500μF (17 kW). The load on the system is changed at t=0.6sec (20kW). The supply currents are nearly sinusoidal, balanced and slightly leading with respect to supply voltages. Fig. 11 and Fig. 12 show the waveforms and harmonic spectra where THD of load current of 76.33% is reduced to 0.71% in supply current. The DSTATCOM controller has regulated DC bus voltage, ac terminal voltage at PCC under varying load conditions and also reduced THD of supply currents to less than the 5% limit.

VII. CONCLUSION

Detailed analysis of a three-phase, four-wire DSTATCOM has been carried out for a configuration realized from three-single phase VSIs. The advantages of this scheme are that independent control of the three VSI's is possible and a cost effective capacitor with lower voltage rating can be utilized. This in-turn reduces the cost and offers an economically viable option as compared to a four leg DSTATCOM. Power quality aspects such as pf correction, voltage regulation, the load balancing and harmonic reduction for linear as well as non-linear loads have been achieved using this DSTATCOM. The performance results have justified the load compensation of the proposed algorithm for DSTATCOM.

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BIOGRAPHIES

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Measurement of Heat in the Stator Windings of an Open Loop Controlled Three Phase Induction Motor Using AC Filters

Y.R. Manjesha [1] Jyothi Balakrishnan[2]

Abstract – A method for the minimization of temperature rise in the stator windings of an induction motor is presented. This is done by reducing the switching noise produced by the pulse width modulated (PWM) inverter that drives the three phase induction motor. The inverter switching noise is reduced by placing an AC filter at the output of the three phase inverter, with the filter neutral point connected to the DC link mid-point of the capacitors. The main use of the AC filter is the significant reduction of the high dv/dt switching noise of the inverter. The common mode (CM) and differential mode (DM) voltages caused by high dv/dt switching noise are also reduced. Considering harmonic content and dv/dt effects on three phase induction motor the temperature rise in the stator windings with and without filter is measured. It is observed that inclusion of the filter substantially reduces the heating of the motor.

Keywords – Harmonics, common mode voltage, differential mode voltage.

I. INTRODUCTION

The voltage/frequency method is used to control the speed of the three phase induction motor. The solid state PWM drive is designed using a microcontroller. The temperature of the stator windings is measured. Solid state PWM drives Fig. 2 used with induction motors have created concerns with regards to the negative impact it has on the insulation system of the motor [11, 12]. This is mainly because the insulation systems are not designed to withstand impulse like voltages produced by the drive. They have been designed to operate solely at power frequency (50/60Hz). Most of the problems that occur due to the use of these drives result from the steep front pulses (high dv/dt) and added harmonic content of the output waveforms, that cause overshoots at the motor terminals [13], increased motor heating [15], and bearing currents [5]. The large overshoots that occur at the terminals result from using long feeders to supply the motor. These overshoots shown in Fig.1, occur because there is a mismatch between the cable impedance and the motor impedance. This mismatch causes the traveling wave produced by the inverter to be reflected back upon itself. The superposition of the reflected wave and the incoming wave can cause spikes of up to two times the nominal voltage that appear at the motor terminals [13].

The increased motor heating is a result of the additional harmonic content found in the PWM waveform compared with that of the sinusoidal 50Hz waveform.

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These harmonics do not contribute to the output power of the motor and are simply converted to heat, which may speed up the thermal degradation of the insulation.

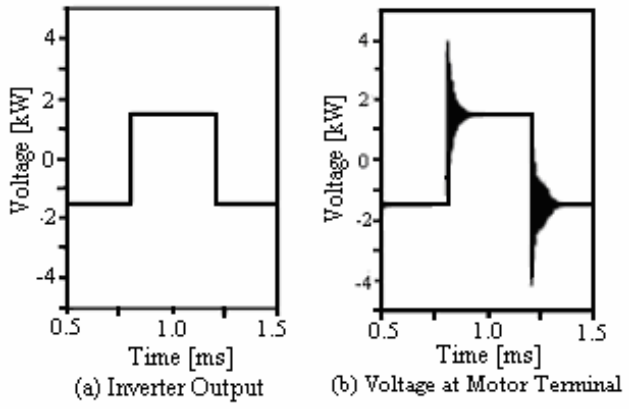

Fig. 1: Inverter output voltage (a) motor terminal voltage (b) motor connected with long feeder.

The PWM inverter uses high speed switching devices such as IGBT's. Due to high speed switching and fast changes in voltages and currents, leads to the following serious problems.

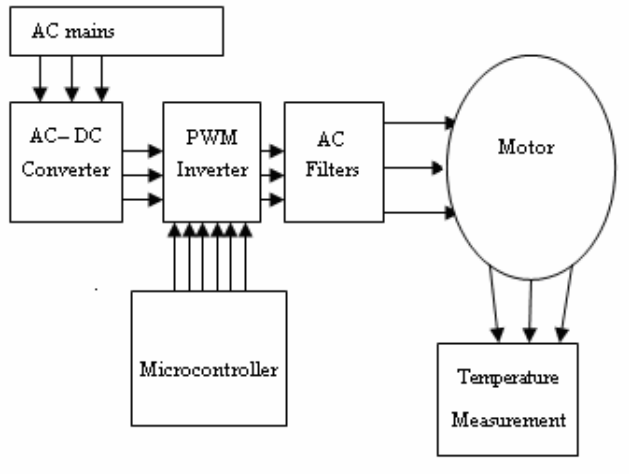

Fig. 2: Three phase induction motor with temperature measurement

1. Ground current flows to earth through stray capacitors inside the motor [1,2].
2. Electromagnetic interference generation [3,6].
3. Generation of shaft voltage and bearing current [7,9].
4. Heating of stator windings
5. Shortening of insulation life of motor [10,13].

Due to the parasitic stray capacitance inside the induction motor and the change in voltage and current caused by

high speed switching high frequency oscillatory common mode (CM) and differential mode (DM) currents are produced at the instant of every switching shown in Fig. 3. This oscillatory current produces a magnetic field and radiates electromagnetic interference (EMI) noise [4, 14] that introduces a bad effect on induction motor windings.
To reduce the impact of the CM and DM noise due to high dv/dt'sa three phase AC filter is introduced between the inverter and the motor shown in Fig. 5. There are several AC filter topologies that have been used to minimize CM or DM noise which causes temperature rise in stator windings of induction motor. Rendusara [15] proposed the use of R-L-C filter in a star connection with the neutral point of the filter connected to the mid-point of the series DC capacitors in the system Fig. 4. This technique reduces the CM, DM voltages and leakage current. The advantage of this AC filter is that it can be connected at the inverter AC terminals without consideration of the AC cable transmission issues [8].

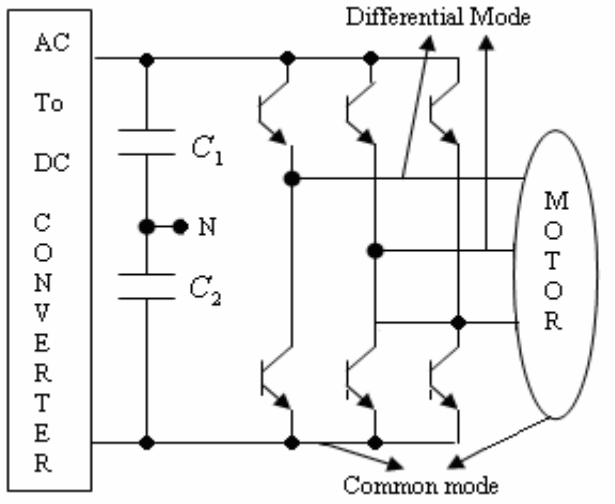

Fig. 3: Inverter drive with common mode and differential mode

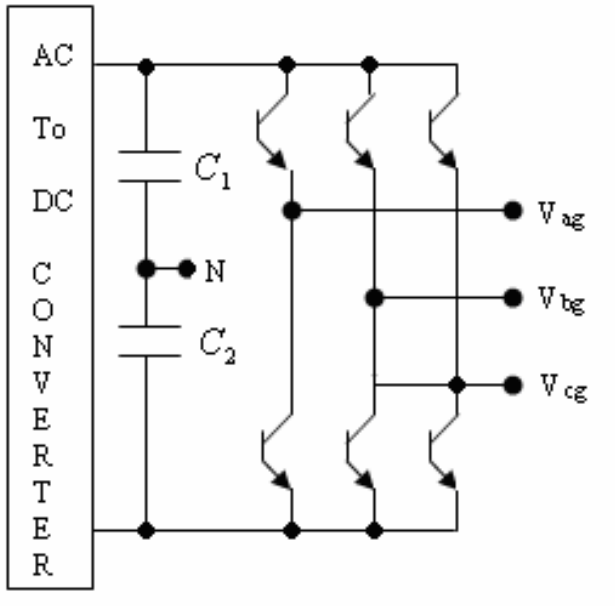

Fig. 4: Motor drive with neutral point

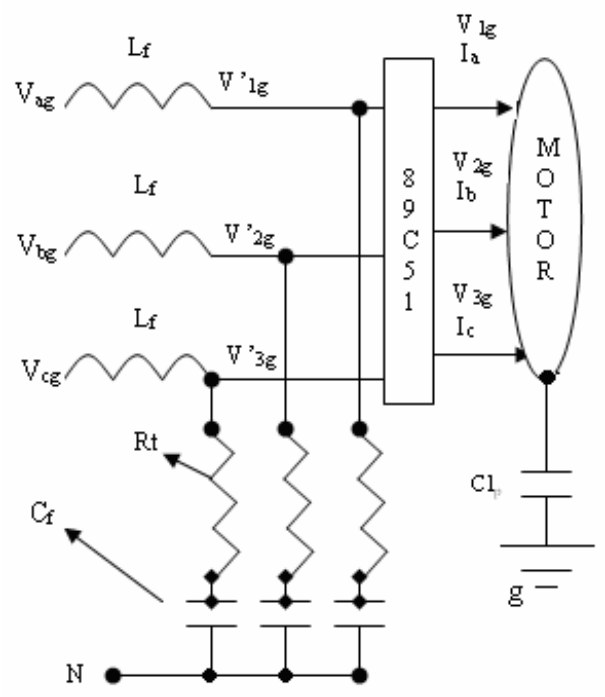

Fig. 5: Filter circuit with neutral point

II. THEORY

The V/F method is used to control the induction motor. The PWM inverter switches at a high frequency of 40 kHz. The three phase induction motor used in the system has a rating of 415V, 50Hz, with a maximum speed of 1300rpm. A variable high torque load is applied to the induction motor which causes the temperature rise in the induction motor. The present system is for a low speed high torque application [17].

III. COMMON MODE VOLTAGE AT MOTOR TERMINALS WITHOUT FILTER

The common mode voltage (V_{cm}) of the induction motor in terms of motor terminal voltages with respect to DC mid-point '0' when no filter is introduced between the inverter and induction motor can be calculated as follows[16].
The common mode voltage (V_{cm}) can be

$$V_{1g} - V_{cm} = R_m I_a + L_m \frac{dI_a}{dt} \quad (1)$$

$$V_{2g} - V_{cm} = R_m I_b + L_m \frac{dI_b}{dt} \quad (2)$$

$$V_{3g} - V_{cm} = R_m I_c + L_m \frac{dI_c}{dt} \quad (3)$$

where V_{1g}, V_{2g} and V_{3g} are the voltages at the motor terminals with respect to ground 'g' and R_m, L_m are the per phase motor winding resistance and inductance respectively.

Adding equations (1), (2) and (3) we obtain

$$V_{1g} + V_{2g} + V_{3g} - 3V_{cm} = R_m + L_m \frac{d}{dt}(I_a + I_b + I_c) \quad (4)$$

Since motor is a balanced system $I_a + I_b + I_c = 0$ therefore the common mode voltage can be expressed as

$$V_{cm} = \frac{V_{1g} + V_{2g} + V_{3g}}{3} \quad (5)$$

The motor terminal voltages with respect to ground 'g' can also be expressed in terms of the DC link middle point '0' of the capacitors as follows.

$$V_{1g} = V_{10} + V_{0g} \quad (6)$$

$$V_{2g} = V_{20} + V_{0g} \quad (7)$$

$$V_{3g} = V_{30} + V_{0g} \quad (8)$$

Therefore

$$V_{cm} = \frac{V_{10} + V_{20} + V_{30}}{3} + V_{0g} \quad (9)$$

In this inverter three out of six IGBT switches are conducting at any given time. The six switching states provide voltage to the motor and alternate between one top switch with two bottom switches on and two top switches with one bottom switch on.

The summation of the voltage at the inverter AC terminals with respect to the DC link mid-point '0' can be expresses as

$$V_{a0} + V_{b0} + V_{c0} = \pm \frac{V_{dc}}{2} \quad (10)$$

The PWM inverter and motor configuration without an AC filter can experience over voltages due to reflections at the motor terminals which can be attributed to the high voltage dv/dt [7]. This voltage may be approximately twice the amount of voltage seen at the inverter terminals given in equation (10). Therefore the motor terminal voltage with respect to DC link mid-point '0' can be expressed as follows.

$$V_{10} + V_{20} + V_{30} = \pm V_{dc} \quad (11)$$

[One top and two bottom switches on or vice versa]
Instantaneous common mode voltage can be expressed as

$$V_{cm}(inst) = \left[\pm \frac{Vd_c}{3} + V_{0g} \right] \quad (12)$$

IV. Common Mode Voltage With An AC Filter

Shows an R-L-C connected between the inverter and the induction motor with connection between the filter neutral 'N' to the DC link mid-point '0' is shown in Fig. 5. This configuration suppresses the high line to line dv/dt voltage (differential mode). The reduction of differential mode dv/dt helps to alleviate the stresses on the motor windings and also suppresses the voltage reflection along the three phase line. With a proper design of the R-L-C filters, all high frequency switching noise is attenuated and provides a differential mode output of nearly sinusoidal line to line voltage at fundamental frequency for the system.

Since the R-L-C filter supplies near sinusoidal voltage to the induction motor the filter output stage voltages (V'_{1g}, V'_{2g}, and V'_{3g}) can be equated to the induction motor terminals voltages, V_{1g}, V_{2g} and V_{3g}. Therefore the common mode voltage at the motor terminals can be expresses as follows.

$$V_{cm} = \frac{V_{1g} + V_{2g} + V_{3g}}{3} = \frac{V'_{1g} + V'_{2g} + V'_{3g}}{3} \quad (13)$$

The voltage relationship between the inverter terminal voltages and the output of the AC filter can be also expressed as

$$V_{ag} - V'_{1g} = L_f \frac{di\,1}{dt} \quad (14)$$

$$V_{bg} - V'_{2g} = L_f \frac{di\,2}{dt} \quad (15)$$

$$V_{cg} - V'_{3g} = L_f \frac{di\,3}{dt} \quad (16)$$

Adding equations (14), (15) and (16) results in

$$(V_{ag} + V_{bg} + V_{cg}) - (V'_{1g} + V'_{2g} + V'_{3h}) = L_f \frac{d(I_a + I_b + I_c)}{dt} \quad (17)$$

$$I_a + I_b + I_c = 0$$

equation (17) becomes

$$(V_{ag} + V_{bg} + V_{cg}) = (V'_{1g} + V'_{2g} + V'_{3g}) \quad (18)$$

Substituting equation (18) into equation (13) Vcm yields

$$V_{cm} = \frac{V_{ag} + V_{bg} + V_{cg}}{3} \quad (19)$$

Each inverter terminal voltages from equation (19) (V_{ag}, V_{bg} and V_{cg}) can also expressed as the sum of its terminal voltage with respect to the DC link mid-point '0' plus the voltage from the mid-point '0' with respect to the system ground.

$$V_{ag} = V_{a0} + V_{0g} \quad (20)$$

$$V_{bg} = V_{b0} + V_{0g} \quad (21)$$

$$V_{cg} = V_{c0} + V_{0g} \quad (22)$$

Substituting equations (20), (22) and (23) in equation (19) yields.

$$V_{cm} = \frac{V_{a0} + V_{b0} + V_{c0}}{3} + V_{0g} \quad (23)$$

By combining the equations (10) and (23) The instantaneous common mode voltage (V_{cm}) for an induction motor an inverter system with R-L-C results in

$$V_{cm}(inst) = \left[\pm \frac{V_{dc}}{6} + V_{0g} \right] \quad (24)$$

[one top and two bottom switches on or vice versa]

V. AC Filter Design

The present set up is for low speed high torque applications of motor. The motor is designed to work at 11.5Hz with a speed of 319 rpm using V/F control method. The R-L-C filter is designed for a cut-off frequency of 11.5Hz to 159Hz.

$$f_c = \frac{1}{2\pi\sqrt{LC}} \quad (25)$$

VI. Experimental Results

The temperature of stator windings of three phase induction motor with control of speed by voltage/frequency technique using microcontroller has been studied. The temperature is recorded without any filter between the inverter and induction motor.

The temperature of stator windings after introducing an AC filter for two different cut-off frequencies, by selecting proper values to L-R-C filter is also measured. Since the

rise in temperature in induction motor is high at low frequency hence the ratings of the induction motor reduced to 95V/11.5Hz. (V/F) to maintain constant torque.

The Experimental Setup is:
V = 95V
F = 11.5Hz
Speed = 319 rpm
Torque load = 0.477Nm
C_1=C_2=1000mF/450VDC

VII. Conclusion

The stator temperature of three phase induction motor is experimentally studied with and without AC filter at the output of the inverter (Fig.6-8). In this experiment we are studying only temperature effects on induction motor, hence the use of an R-L-C filter with its neutral connected to DC link mid-point '0' proved to be advantageous for the induction motor and magnetic bearing system by reducing the common mode (CM) and differential mode (DM) noise without affecting the motor control. Noise in the motor system caused by the DC to AC inverter high dv/dt switching is reduced by designing the values of the R-L-C filters between 11.5Hz to 159 Hz. Voltage stress and voltage doubling effect at the motor terminals have been considerably reduced, which reduces the temperature in the stator windings of three phase induction motor.

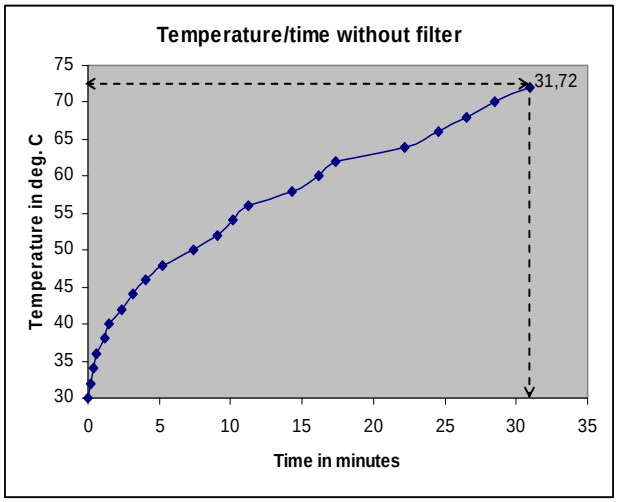

Fig. 6: Temperature/time curve without filter.

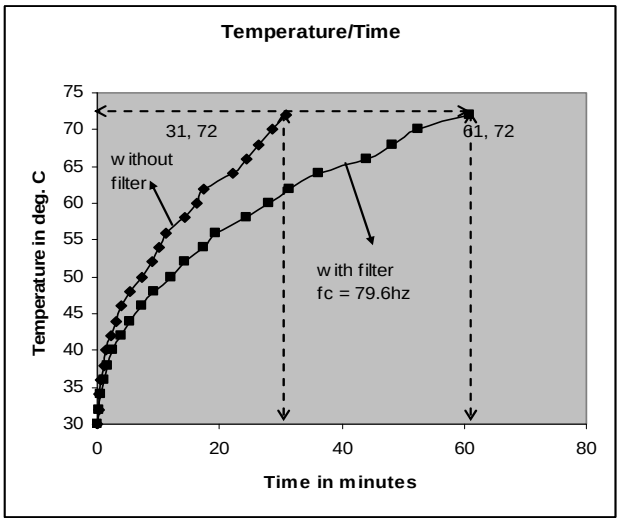

Fig. 7: Selecting L_f = 90mH, C_f = 100 μF, f_c = 79.6Hz.

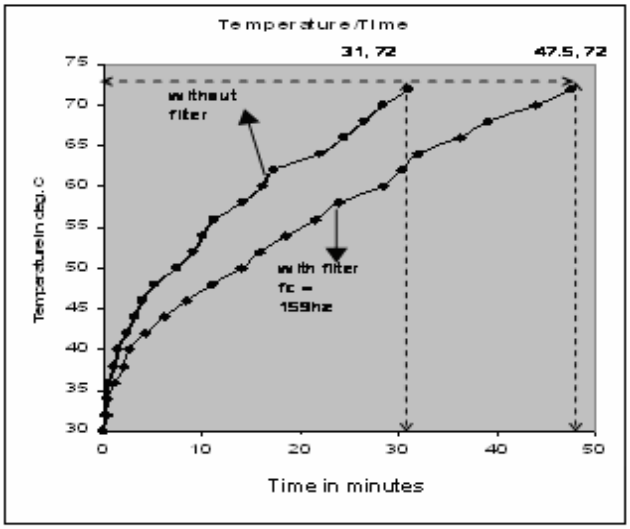

Fig. 8: Selecting L_f = 90 mH, C_f = 100 μF, f_c =159 Hz.

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BIOGRAPHIES

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Particle Swarm Optimization Based Power System Stabilizer to Reduce Generator Rotor Oscillations

A. Jeevanandham[1] K. Thanushkodi[2]

Abstract –A classical lead-lag power system stabilizer is used for demonstration in this paper. Initially single first-order phase compensation block is considered. The stabilizer parameters are selected in such a manner to damp the rotor oscillations. The problem of selecting the stabilizer parameters is converted to a simple optimization problem with an eigen value based objective function and it is proposed to employ particle swarm optimization for solving optimization problem. The objective function allows the selection of the stabilizer parameters to optimally place the closed-loop eigen values in the left hand side of the complex s-plane. The effectiveness of the stabilizer tuned using the above technique, in enhancing the stability of power system. Stability is confirmed through eigen value analysis and simulation of results for the best performance of the system.

Keywords – Power system stability, rotor oscillations, robust control, particle swarm optimization

I. INTRODUCTION

During changes in operating conditions, oscillations of small magnitude and low frequency often persist for long period of time and in some cases even present limitations on power transfer capability. Power system stabilizer (PSS) is designed to damp the low frequency oscillations of power system [1].

PSS is used to add damping to the generator rotor oscillations by controlling its excitation using auxiliary stabilizing signals. The widely used conventional power system stabilizer (CPSS) is designed using the theory of phase compensation and introduced as a lead-lag compensator [7].

An inter connected power system, depending on its size, has hundreds to thousands of modes of oscillation. In the analysis and control of system stability, two distinct types of system oscillations are usually recognized. One type is associated with units at a generating station swinging with respect to the rest of the power system. Such oscillations are referred to as local plant mode oscillations. The frequencies of these oscillations are typically in the range of 0.8 to 2.0 Hz. The second type of oscillations is associated with the swinging of many machines in one part of the system against machines in the other parts. These are referred to as inter area mode oscillations, and have frequencies in the range of 0.1 to 0.7 Hz.

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The basic function of PSS is to add damping to both types of system oscillations.
Other modes which may be influenced by PSS include torsional modes and control modes such as the exciter mode associated with the excitation system and the field circuit [5]. The over all excitation control system is designed so as to maximize the damping of the local plant mode as well as inter-area mode oscillations with out compromising the stability of other modes and to enhance system transient stability. Input to PSS is rotor speed deviation which results damping torque.

II. CONTROLLER DESIGN

Damping torque is produced to overcome rotor oscillation. The action of a PSS is to extend the angular stability limits of a power system by providing supplemental damping to the oscillation of synchronous machine rotors through the generator excitation [3].

Controller is designed to compensate lag between exciter input (ΔV_s) and electrical torque (ΔT_{pss}).

$$\frac{\Delta T_{PSS}}{\Delta V_S} = K\angle -\theta \qquad (1)$$

The amount of damping introduced depends on the gain of $\Delta\omega_r$ transfer function at that particular fr ΔV_S y of oscillation.

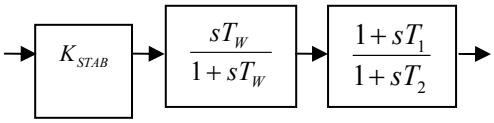


Fig. 1: Lead – lag power system stabilizer

A. Phase Lead Compensation

To provide damping, the stabilizer must produce a component of electrical torque which is in phase with speed variations. Therefore, the PSS transfer function should have an appropriate phase-lead characteristics to compensate for the phase lag between the exciter input and the electrical torque.

The phase characteristic has to be compensated changes with system conditions. Therefore, a compromise must be made and a characteristic acceptable for a desired range of frequencies (normally 0.1 to 2.0 Hz) and for different system conditions is selected. This may result in less than optimum damping at any one frequency. Generally, slight under compensation is preferable to overcompensation so that both damping and synchronizing torque components are increased.

B. Stabilizing Signal Washout

The signal washout function is a high pass filter which removes dc signals, and without it steady changes in speed would modify the terminal voltage. The washout time constant is in the range of 1 to 20 seconds. For local mode oscillation, a wash out of 1 to 2 sec is satisfactory. From the view point of low frequency inter area oscillations a washout time constant of 10 sec or higher may be required in order to reduce phase lead at low frequencies.

C. Stabilizer Gain

The stabilizer gain (K_{STAB}) is chosen by examining the effect for a wide range of values. Ideally, the stabilizer gain should be set at a value corresponding to maximum damping. Gain is set to a value which results in satisfactory damping of the critical system mode(s) without compromising the stability of other modes, or transient stability, and which does not cause excessive amplification of stabilizer input signal noise.

D. Stabilizer Output Limits

In order to restrict the level of generator terminal voltage fluctuation during transient conditions, limits are imposed on the PSS output. The effect of the two limits is to allow maximum forcing capability while maintaining the terminal voltage within the desired limits [3].

III. Problem Formulation

In this section, the eigen value-based objective function used to robustly select the PSS parameters [2], and the optimization problem solved with particle swarm optimization.

Consider the problem of determining the parameters of a stabilizer that relatively stabilizes a family of N plants,

$$\dot{X}(t) = A_k X(t) + B_k U(t); \quad k = 1,2,3,...N \tag{2}$$

where $\dot{X}(t) \in R^n$ is the state vector and $X(t) \in R^m$ is the control vector.

Very often, the closed-loop modes are specified to have some degree of relative stability. In this case closed-loop eigen values are constrained to lie to the left of a vertical line corresponding to a specified damping factor.

A necessary and sufficient condition for the set of plants in equation (2) to be simultaneously relatively stabilizable with a single control law is that the eigen values of the closed-loop system lie in the left-hand side of a vertical line in the complex s-plane. This condition motivates the following approach for determining the parameters of the PSS.

Select the parameters of the PSS to minimize the following objective function:

$$J = \max\left\{\mathrm{Re}\left(\lambda_{k,i}\right) + \beta\right\};\ k = 1,2,3,...N;\ i = 1,2,...n \tag{3}$$

where $\lambda_{k,i}$ is i^{th} closed loop eigen value of the k^{th} plant and β is relative stability factor. Subject to the constraints that finite bounds are placed on the stabilizer parameters.

In this paper instead of N number of plants, single-machine-infinite-bus system is considered. The objective function can be modified as,

$$J = \max\left\{\mathrm{Re}\left(\lambda_k\right) + \beta\right\} \tag{4}$$

The relative stability is determined by the value of β as shown in Fig. 2

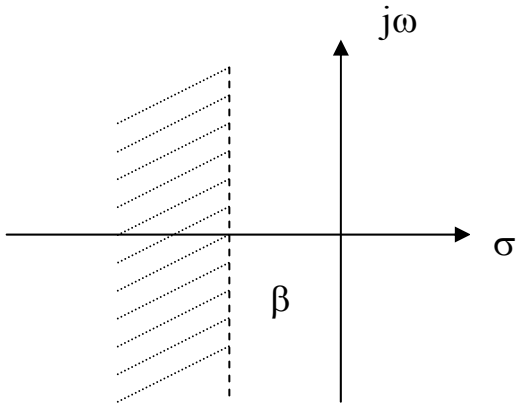


Fig. 2: Region in the left-hand side of a vertical

Plainly, if a solution is found such that $J < 0$, then the resulting parameters simultaneously relatively-stabilize the collection of plants. The existence of a solution is verified numerically [2] by minimizing J.

IV. System Model

In this steady single-machine-infinite-bus power system is considered [9]. The supplementary stabilizing signal considered is one proportional to speed [6]. A widely used conventional PSS is considered throughout the study.

The transfer function of PSS with single phase compensation block is

$$\frac{\Delta V_S}{\Delta \omega_r} = K_{STAB} \frac{sT_W}{1+sT_W} \frac{1+sT_1}{1+sT_2} \tag{5}$$

The first term is stabilizer gain. The second term is washout term with a time lag T_w. The third term is a lead compensation [3] to improve the phase lag through the system. The numerical values of T_w, T_2 and system data are given in Appendix I. The remaining parameters namely K_{STAB} and T_1 are assumed to be adjustable parameters. The optimization problem is selection of these PSS parameters easily and accurately. The optimization problem can be solved using the particle swarm optimization. The PSO algorithm in explained in Appendix II.

For a given operating point, the power system is linearized around the operating point, the eigen values of the closed-loop system are computed, and the objective function is evaluated. It is worth mentioning that only the system electromechanical modes are incorporated in the objective function. The bounds on the parameters used in the PSO are given in Appendix I.

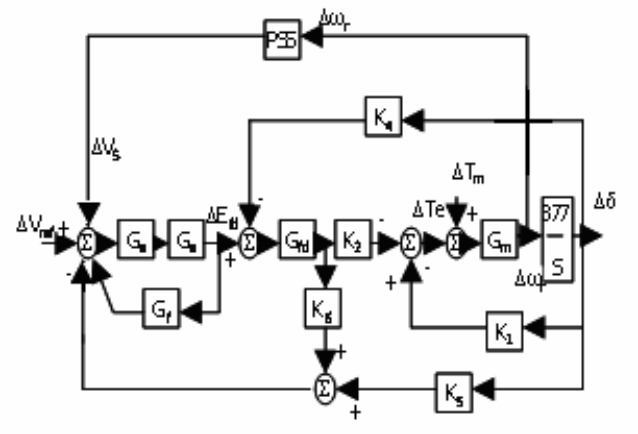


Fig. 3: Block diagram of AVR with PSS

The system with multivariable state space model [11] for individual generator may be considered in a multimachine system and the PSS parameters can be tuned by using the PSO. In our case the state space model for SMIB system [9] is considered.

V. Particle Swarm Optimization

Similar to evolutionary algorithms, the PSO technique conducts searches using a population of particles, corresponding to individuals. In a PSO system [10], particles change their positions by flying around in a multidimensional search space until a relatively changed position has been encountered, or until computational limitations are exceeded.

The following are the advantages of PSO [8] over other traditional optimization techniques.

- PSO is a population based search algorithm. This property ensures it to be less susceptible to getting trapped on local minima.
- PSO uses payoff (performance index or objective function) information to guide the search in the problem space.
- PSO uses probabilistic transition rules and not deterministic rules. Hence, PSO is a kind of stochastic optimization algorithm that can search a complicated and uncertain area.

A. Particle X(t):

It is a candidate solution presented by an m-dimensional real-valued vector, where m is the number of optimized parameters.

B. Population pop(t):

It is a set of n particles at time *t*.
(i.e. pop(t) = $[X_1(t), X_2(t), \ldots, X_n(t)]^T$)

C. Swarm:

It is disorganized population of moving particles that tend to cluster together while each particle seems to be moving in a random direction.

D. Particle velocity V(t):

It is the velocity of the moving particles represented by an *m*-dimensional real valued vector. At the time *t*, the *j*th particle velocity $V_j(t) = [v_{j,1}(t), v_{j,2}(t),\ldots, v_{j,m}(t)]$, where $v_{j,k}(t)$ is the velocity component of *j*th particle with respect to the *k*th dimension.

E. Individual best $X^*(t)$:

As the particle moves through the search space, it compares its fitness value at the current position to the best fitness value it has ever attained at any time up to the current time. The best position that is associated with the best fitness encountered so far is called is called individual best $X^*(t)$. For each particle in the swarm, $X^*(t)$ can be determined and updated during the search. In a minimization problem objective function *J*, the individual best of the *j*th particle $X_j^*(t)$ is determined so that $J(X_j^*(t)) \le J(X_j^*(\tau)), \tau \le t$. For simplicity, assume that $J_j^* = J(X_j^*(t))$. For the *j*th particle, individual best can be expressed as $X_j(t) = [x^*_{j,1}(t), x^*_{j,2}(t),\ldots, x^*_{j,m}(t)]$.

F. Global best $X^{**}(t)$:

It is the best position among all of the individual best positions achieved so far. Hence, the global best can be determined such that $J(X^{**}(t)) \le J(X_j^*(t)), j = 1,2,\ldots n$. For simplicity, assume that $J^{**} = J(X^{**}(t))$.

G. Stopping criteria:

These are the conditions under which the search process will terminate. In this study, the search will terminate if one of the following criteria is satisfied,
a) The number of iterations since the last change of the best solution is greater than a prespecified number
b) The number of iterations reaches the maximum allowable number.

The particle velocity in the kth dimension is limited by some maximum value, v_k^{max}. This limit enhances the local exploration of the problem space and it realistically simulates the incremental changes in human learning. The maximum velocity in the kth dimension is characterized by the range of the kth optimized parameter and given by

$$v_k^{\max} = \frac{\left(x_k^{\max} - x_k^{\min}\right)}{N}$$

where *N* is a chosen number of intervals in the kth dimension.

VI. Simulation Results

In this part of the study, a single machine is connected to infinite bus through a transmission line, and operating at different loading conditions [4], is considered. The linearized model of this system, voltage regulator and exciter included [10] is considered.

The constants K_1 to K_6, with the exception of K_3, which is only a function of the ratio of impedance, are dependent on the actual real power (P) and reactive power (Q) loading as well as the excitation levels in the machine.

The operating points are selected based on the different loading conditions. The simultaneous damping enhancement of demonstrated by considering five different loading conditions.

The operating points were selected randomly as follows:
(Po , Qo) = (0.9, 0.3) ; (0.8, -0.1); (0.5,0.5) ; (0.6, -0.2)
(1.0, 0.6)

The eigen values are found by transferring the transfer function of the system data into state space model.

The eigen values of the system at the five operating points considered, with out PSS are,
1. 0.4981 ± 6.6288i, -33.6805, -17.3597
2. 0.7513 ± 7.3702i, -11.5526, -39.9942
3. 0.0283 ± 5.3580i, -25.0504 ± 9.1822i
4. 0.1936 ± 6.9157i, -10.7786, -39.6528
5. 0.5410 ± 6.1171i, -21.6341, -29.4919

From the eigen values it is clear that the system is unstable due to its location in the right half of the *s* – plane.

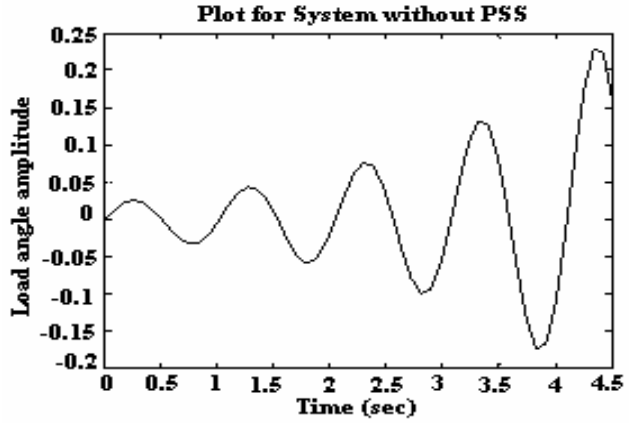
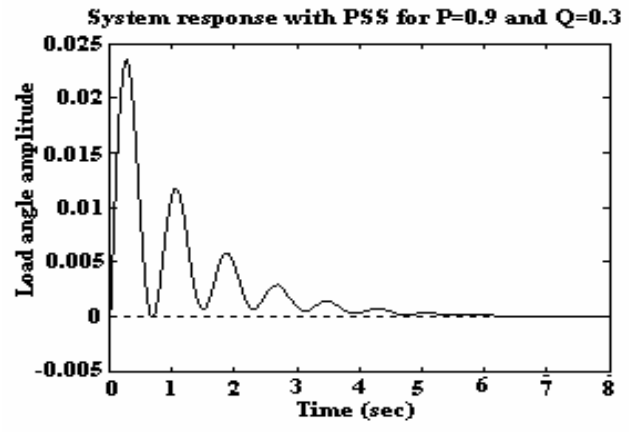


Fig. 4: Response of the system without PSS

For the system to be stable the real part of eigen value should be located in the in the left hand side of s-plane.

The objective function *J* is optimized with the PSO and *N*=5 to shift the electromechanical mode of each of the five systems to the left of the vertical line defined by β = -2.2.

The eigen values of the five systems, with PSS are
1. -34.1670±5.0796i, -9.9855, -0.9887± 7.7731i,-0.7644
2. -37.4972,-35.6751, -0.5533±9.3491i, -6.0033,-0.7792
3. -29.0306±7.0224i, -20.4992,-0.8755±5.6109i,-0.7500
4. -36.4206±0.9044i, -1.3020±9.2146i, -4.8165, -0.7998
5. -33.0536±5.8900i,-12.5555, -0.8183±6.9006i,-0.7620
All the eigen values of the system were located in the left half of the *s* – plane. So the system will be stable.



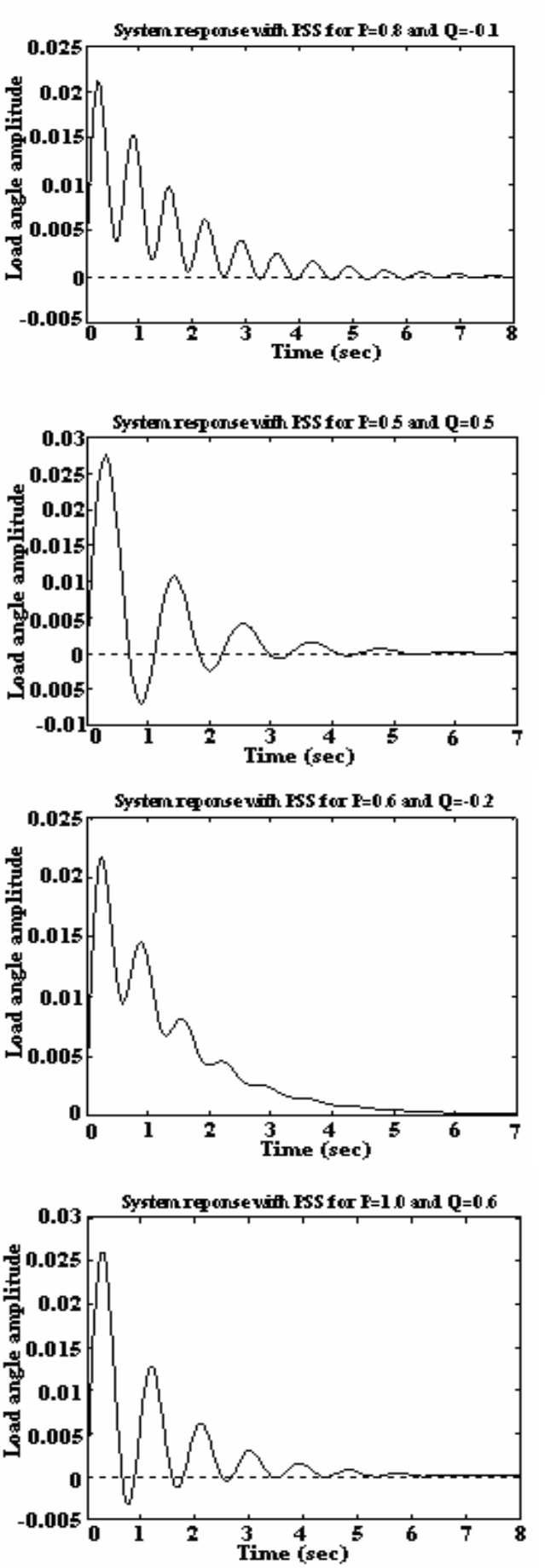


Fig. 5: Response of the system with PSS using particle swarm optimization

Fig. 5 shows response of the system with power system stabilizer for various operating conditions whereas their parameters were tuned by using Particle Swarm Optimization (PSO). It is indicating simultaneous improvement in the response of the five systems.

The above two techniques can be compared as shown in Table 1.

Table 1: Comparison between conventional method and particle swarm optimization

Loading Condition (*Po* , *Qo*)	Conventional Method		Particle Swarm Optimization	
	Settling Time in Sec.	Peak Amp.	Settling Time in Sec.	Peak Amp.
0.9, 0.3	20.8	0.0443	4.51	0.0236
0.8, -0.1	7.6	0.0313	6.32	0.0211
0.5, 0.5	5.58	0.0287	4.92	0.0275
0.6, -0.2	6.96	0.0272	5.06	0.0218
1.0, 0.6	5.09	0.0324	4.99	0.026

From the above comparison the Particle swarm optimization technique is having lower settling time, lower peak amplitude and lesser computational time than conventional method. Moreover by using PSO the eigen values are located far away in the left hand side of s-plane to make the system more stable. So tuning of PSS parameters by using PSO is more optimal than conventional technique.

VII. CONCLUSION

The use of PSO to design robust power system stabilizers for power systems working at various operating conditions are investigated in this paper. The problem of selecting the PSS parameters, which simultaneously improve the damping at various operating conditions, is converted to an optimization problem with an eigen value-based objective function which is solved by both conventional and PSO techniques.

The objective function is presented allowing the robust selection of stabilizer parameters that will optimally place the closed-loop eigen values in the left hand side of a vertical line in complex s-plane. By comparing the above two optimization techniques, it is found that Particle Swarm Optimization is better than Conventional method in tuning the parameters of the Power system stabilizer, to reduce intra and inter area rotor oscillations over a wide range of operating conditions.

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APPENDIX I

SYSTEM DATA

A. Single- Machine- Infinite- Bus System:

$$G_m = \frac{1}{2H_S + K_D};\quad G_A = \frac{K_A}{sT_A + 1};\quad G_e = \frac{1}{sT_E + 1}$$

$$G_f = \frac{sK_f}{1 + sT_F};\qquad G_{fd} = \frac{K_3}{1 + sT'_{do}K_3}$$

B. Machine (p.u)

$x_d = 1.7$; $x_d' = 0.254$; $x_q = 1.64$; $\omega_0 = 120\,\pi$ rad/s ;
$T_{do}' = 5.9$ sec ; $K_D = 0$; H = 2.37 sec

C. Transmission Line (p.u)

$r_e = 0.02$; $x_e = 0.4$

D. Exciter and Stabilizer

$K_A = 400$; $T_A = 0.05$ sec ; $K_F = 0.025$
$T_F = 1.0$ sec ; $K_E = -0.17$; $T_E = 0.95$ sec
$T_W = 10$ sec ; $T_2 = 0.0227$ sec
Bounds for the stabilizer adjustable gain and time constants are [0.01, 10] and [0.03, 1.0] respectively.

APPENDIX II

PARTICLE SWARM OPTIMIZATION

Step (1): Set the time counter $t = 0$ and generate random n particles, $\{X_j(0),\ j = 1,2,\ldots n\}$, where $X_j(0) = [x_{j,1}(0), x_{j,2}(0), \ldots x_{j,m}(0)]$. $x_{j,k}(0)$ is generated by randomly selecting a value with uniform probability over the kth optimized parameter search space $[x_k^{min}, x_k^{max}]$.Generate randomly initial velocities of all particles, $\{V_j(0),\ j = 1,2,\ldots n\}$, where $V_j(0) = [v_{j,1}(0), v_{j,2}(0), \ldots v_{j,m}(0)]$. $v_{j,k}(0)$ is generated by randomly selecting a value with uniform probability over the kth optimized parameter search space $[-v_k^{max}, v_k^{max}]$. Each particle in the initial population is evaluated using the objective function, J. For each particle, set $X^*_j(0) = X_j(0)$ and $J^*_j = J_j$, $j = 1,2,\ldots,n$. Search for the best value of objective function J_{best}. Set the particle associated with J_{best} as the global beat, $X^{**}(0)$, with an objective function of J^{**}. Set the initial value of the inertia weight $w(0)$.

Step (2): Update the time counter $t = t+1$.

Step (3): Update the inertia weight $w(t) = \alpha\, w(t-1)$.

Step (4): Using the global best and individual best, the jth particle velocity in the kth dimension is updated according to the following equation:

$$v_{j,k}(t) = w(t)v_{j,k}(t-1) + c_1 r_1 (x^*_{j,k}(t-1) - x_{j,k}(t-1) + c_2 r_2 (x^{**}_{j,k}(t-1) - x_{j,k}(t-1))$$

where c_1 and c_2 are positive constants and r_1 and r_2 are uniformly distributed random numbers in [0,1].

Step (5): Based on the updated velocities, each particle changes its position according to the following equation:

$$x_{j,k}(t) = v_{j,k}(t) + x_{j,k}(t-1)$$

Step (6): Each particle is evaluated according to the updated position. $J_j < J^*_j$, $j=1,2,\ldots,n$, then update individual best as $X^*_j(t) = X_j(t)$ and $J^*_j = J_j$, and go to step 7; else go to step 7.

Step (7): Search for the minimum value J_{min} among J^*_j, where min is the index of the particle with minimum objective function value, i.e., min ϵ $\{j; j=1,2,\ldots,n\}$. If $J_{min} < J^{**}$ then update global best as $X^{**} = X_{min}(t)$, and $J^{**}=J_{min}$ and go to step 8; else go to step 8.

Step (8): If one of the stopping criteria is satisfied, then stop, or else go to step 2.

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BIOGRAPHIES

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Three-Phase Four-Wire DSTATCOM with Reduced Switches for Power Quality Improvement

Bhim Singh[1] P. Jayaprakash[2] D.P. Kothari[3]

Abstract – In this paper, a two-leg VSC (voltage source converter) integrated with a star/hexagon transformer is used for the power quality improvement in three-phase four-wire distribution system. The primary winding of the transformer is star connected and it provides a path to the zero sequence fundamental as well as harmonics neutral currents. The secondary windings of the transformer are connected in hexagon manner and it provides isolation to the two-leg VSC. In order to optimise the voltage rating of the two-leg VSC, the secondary winding of the transformer is suitably designed. The proposed DSTATCOM (Distribution Static Compensator) provides the voltage regulation or power factor correction by reactive power compensation, harmonics elimination, load balancing and neutral current compensation in three-phase four-wire distribution system. This topology has the advantages of the use of 'off the shelf' two-leg VSC, reduced size and cost. The rating of the transformer remains same when it is compensating the neutral current due to unabalance in the load. The performance of the proposed DSTATCOM system is validated through simulations using MATLAB software with its Simulink and Power System Blockset (PSB) toolboxes.

Keywords - Power quality, DSTATCOM, H-bridge VSC, star/hexagon transformer, neutral current compensation

I. INTRODUCTION

The power quality problems in the three-phase four-wire distribution systems are severe mainly due to the proliferation of different types of non-linear loads, unplanned expansion of the distribution system etc. These power quality problems include high reactive power burden, harmonic currents, load unbalance and excessive neutral current [1-4]. The power quality aspects are governed by the various standards such as the IEEE-519 standard [5]. Some remedies to these power quality problems are reported in the literature [2-4] and the group of controllers used in the distribution system is known as custom power devices (CPD) which include the DSTATCOM (distribution static compensator), DVR (dynamic voltage restorer) and UPQC (unified power quality conditioner). These are used for compensating the power quality problems in the current, voltage and both current and voltage respectively. The DSTATCOM is developed and installed in the distribution system for power quality improvement [6].

Three-phase four-wire distribution systems are used to supply single-phase low voltage loads. The typical loads may be computer loads, lighting ballasts, small rating adjustable speeds drives (ASD) in air conditioners, fans, refrigerators and other domestic and commercial appliances etc. These loads may create problems of harmonics in the supply current as well as excessive neutral current. The neutral current consists of mainly third harmonics currents [3]. The zero- sequence neutral current gets a path through the neutral conductor. The unbalanced single-phase loads result in high neutral current. Three-phase four-wire shunt compensators are reported in the literarure [7-8] for neutral current compensation along with harmonic elimination and load balancing. The use of split capacitors with 2-leg VSC (voltage source converter) is used for compensation in three-phase three-wire system [9-10]. Some of the topologies of three-phase four-wire DSTATCOM for the mitigation of the neutral current along with power quality compensation in the supply current are four-leg VSC (voltage source converter), three single phase VSC, three-leg VSC with split capacitors [3], three-leg VSC with zig-zag transformer [7], three-leg VSC with neutral terminal at the positive or negative terminal of dc bus [8]. The application of a zig-zag transformer for reduction of the neutral current has the advantages due to passive compensation, rugged and less complex over the active compensation techniques [7].

In this paper, a new topology of DSTATCOM is proposed in which a two-leg VSC along with a star/hexagon transformer is able to perform required compensations for a three phase four wire system. Moreover, the star/hexagon transformer is suitably designed for mmf (magnetic motive force) balance. The star/hexagon transformer mitigates the neutral current and the H-bridge VSC compensates harmonic current, reactive power and balances the load. In order to optimize the voltage rating of the H-bridge VSC, the star/hexagon transformer is designed for integrating the DSTATCOM with the secondary winding of the transformer. The dynamic performance is studied for voltage regulation and power factor correction mode of the DSTATCOM using MATLAB software with its Simulink and PSB (power system blockset) tool boxes.

II. PROPOSED DSTATCOM

The three-phase four-wire DSTATCOM is used for reactive power and harmonics currents compensation along with load balancing and neutral current elimination. Fig. 1 shows the power circuit of proposed H-bridge VSC integrated with star/hexagon transformer as DSTATCOM. The linear and non-linear, balanced and unbalanced loads are connected at the PCC. The star/hexagon transformer connected at the load terminal provides a path for zero sequence harmonics and fundamental currents. A set of

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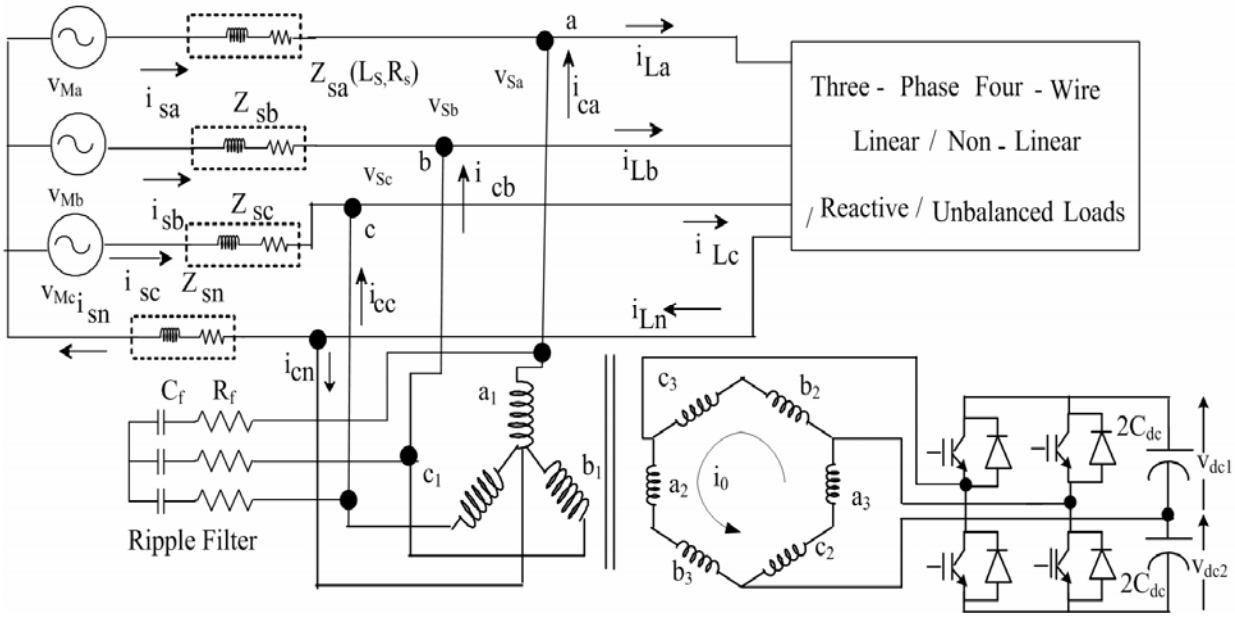

Fig. 1: Proposed Integrated 3-leg VSC with star/hexagon transformer based DSTATCOM in the distribution system.

secondary windings are designed in the star/hexagon transformer for connecting the H-bridge VSC. The VSC consists of four insulated-gate bipolar transistors (IGBTs) and two dc capacitors.

This transformer provides an isolation to the VSC as well as the suitability of selecting an 'off the shelf' H-bridge VSC for this application. In the zero voltage regulation (ZVR) mode of operation, DSTATCOM injects a current I_c, such that the voltage at PCC (V_S) and the source voltage (V_M) are in the locus of same circle.

A. Star/Hexagon Transformer

The hexagon connected secondary winding of the transformer provides a path for the zero sequence fundamental current and harmonic currents and hence offers a path for the neutral current when connected in shunt at PCC. The voltage across each primary winding is the phase voltage and the H-bridge VSC is connected to this transformer as shown in Fig. 2(a). The volatge rating of the star/hexagon transformer windings are designed [11] as shown below.

The phasor diagram shown in Fig. 2(b) gives the following relations to find the turns ratio of windings. If V_a, V_b and V_c are the per phase voltages across each winding and V_{ca} is the resultant voltage, then

$$V_{ca} = K_1 V_a - K_2 V_c \tag{1}$$

where K_1 and K_2 are the fraction of winding in the phases. Considering $V_a = V\angle 0°$ and $V_{ca} = \sqrt{3}V\angle 30°$, then from (1),

$$\sqrt{3}V\angle 30° = K_1 V\angle 0° - K_2 V\angle -120° \tag{2}$$

one gets, $K_1 = 1$, $K_2 = 1$

The line voltage is, $V_{ca} = 200V$, then

$$V_a = V_b + V_c = 200/\sqrt{3} = 115.50V \tag{3}$$

Hence, three numbers of single-phase transformers of each of rating 5kVA, 240V/120V/120V are selected.

B. H-Bridge VSC

The DSTATCOM uses a two- leg, H-bridge, PWM controlled *IGBTs* based VSC. The rating of the switches is based on the voltage and current rating of the compensation system. For the considered load given in Appendix, the rating of the VSC for power factor correction by reactive power compensation is found to be 12 *kVA*. The selection of dc bus voltage, dc bus capacitor, ac inductor and the ripple filter are selected as per the design of VSC for the shunt compensator [12].

C. Control of DSTATCOM

There are many theories available for the generation of reference source currents for the control of VSC of DSTATCOM for three phase four wire system in the literature viz. instantaneous reactive power theory (p-q theory), synchronous reference frame theory, power balance theory etc [13]. The synchronous reference frame theory based method is used for the control of H-bridge VSC. A block diagram of the control scheme is shown in Fig. 3. The load currents (i_L), the PCC voltages (v_s) and dc bus voltage (v_{dc1}, v_{dc2}) of DSTATCOM are sensed as feedback signals. The loads currents in the three-phases are converted into the d-q-0 frame using the Park's transformation as in eqn. (4).

$$\begin{bmatrix} i_{Ld} \\ i_{Lq} \\ i_{L0} \end{bmatrix} = \frac{2}{3}\begin{bmatrix} \cos\theta & -\sin\theta & \frac{1}{2} \\ \cos\left(\theta-\frac{2\pi}{3}\right) & -\sin\left(\theta-\frac{2\pi}{3}\right) & \frac{1}{2} \\ \cos\left(\theta+\frac{2\pi}{3}\right) & \sin\left(\theta+\frac{2\pi}{3}\right) & \frac{1}{2} \end{bmatrix}\begin{bmatrix} i_{la} \\ i_{lb} \\ i_{lc} \end{bmatrix} \tag{4}$$

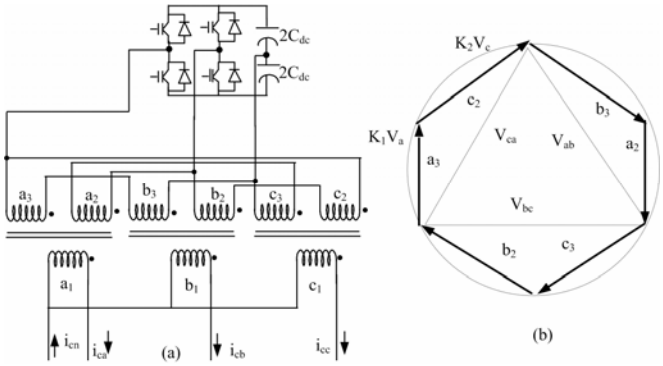

Fig. 2: (a)Star/hexagon transformer and the H-bridge VSC for operation as DSTATCOM (b) phasor diagram

A three-phase PLL (phase locked loop) is used to synchronise these signals with the PCC voltage. These d-q current components are then passed through low pass filters to extract the d_c components of i_d and i_q. The error between the reference dc capacitor voltage and the sensed dc bus voltage of DSTATCOM is given to a PI (proportional-integral) controller and its output voltage is considered as the loss component of the current (i_{loss}) and is added to the dc component of i_d.

$$i_{loss(n)} = i_{loss(n-1)} + K_{pd}(v_{de(n)} - v_{de(n-1)}) + K_{id} v_{de(n)} \quad (5)$$

where, $v_{de(n)} = v_{dc}^{*} - v_{dc(n)}$ is the error between the reference (v_{dc}*) and sensed (v_{dc}) dc voltage at the nth sampling instant. K_{pd} and K_{id} are the proportional and the integral gains of the dc bus voltage PI controller.

The error between the difference of the dc bus capacitors voltages and its reference zero value is given to another PI controller and the output (i_{equal}) is also added to the dc component of i_d.

The reference d-axis supply current is therefore as,

$$i_d^{*} = i_{d\,dc} + i_{loss} + i_{equal} \quad (6)$$

Similarly, a third PI controller is used to regulate the PCC voltage. The amplitude of PCC voltage and its reference value are fed to a PI controller and the output of the PI controller is added with the dc component of i_q because this is estimated as the quadrature component of current for regulating the ac voltage.

$$i_{qr(n)} = i_{qr(n-1)} + K_{pq}(v_{te(n)} - v_{te(n-1)}) + K_{iq} v_{te(n)} \quad (7)$$

where, $v_{te(n)} = V_S^{*} - V_{S(n)}$ denotes the error between reference (V_S *) and actual ($V_{S(n)}$) terminal voltage amplitudes at the nth sampling instant. K_{pq} and K_{iq} are the proportional and the integral gains of the PCC voltage PI controller. The reference q-axis supply current is as

$$i_q^{*} = i_{qdc} + i_{qr} \quad (8)$$

The control strategy is to regulate the PCC voltage, elimination of harmonics in load currents and the load balancing. The resultant d-q-0 currents are again converted into the reference three-phase supply currents using the reverse Park's transformation. The reference currrents in two phases are used for the control of the H-bridge VSC. The sensed and reference supply currents are compared in those two phases before comparing with a triangular carrier signal to generate the gating signals for four switches. For power factor correction of the load, the PCC voltage PI controller is set as zero in the control algorithm of DSTATCOM.

III. MATLAB MODELLING OF DSTATCOM SYSTEM

The H-bridge VSC and the star/hexagon transformer based DSTATCOM interfaced to a three phase four wire system is modeled and simulated using the MATLAB and its Simulink and PSB toolboxes. The DSTATCOM system shown in Fig. 1 is modeled in MATLAB with its Simulink and PSB toolboxes. The load considered is a lagging power factor and non-linear loads. The ripple filter is connected to the VSC of the DSTATCOM for filtering the ripple in the terminal voltage. The system data are given in Appendix. The multi-winding transformer model avilable in the PSB is used for modelling the star/hexagon transformer.

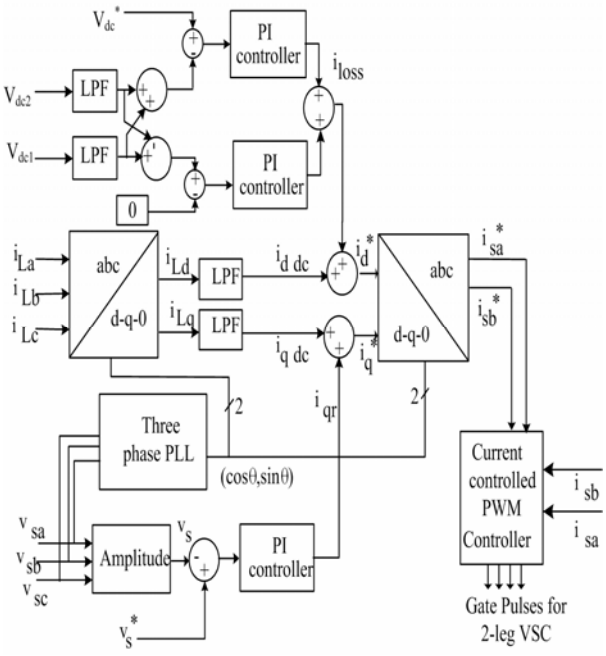

Fig. 3: Control algorithm for the H-bridge VSC

The control algorithm for the DSTATCOM is also modelled in MATLAB. The reference supply currents are derived from the sensed PCC voltages (v_s), load currents (i_L) and the dc bus voltages of DSTATCOM (v_{dc1}, v_{dc2}). A PWM current controller is used over the reference and sensed supply currents to generate the gating signals for the IGBT of the VSC of the DSTATCOM.

IV. RESULTS AND DISCUSSION

The performance of DSTATCOM consisting of H-bridge VSC and the star/hexagon transformer for PCC voltage regulation along with neutral current compensation and load balancing of a three-phase four–wire load is shown in Fig. 4. At 1.8 sec, the load is changed to two-phase load and again to single-phase load at 1.86 sec. These loads are applied again at 1.94 sec and 2.0 sec respectively. The voltages at PCC (v_s), balanced supply currents (i_s), load currents (i_{La}, i_{Lb}, i_{Lc}), compensator currents (i_C), supply neutral current (i_{sn}), load neutral current (i_{Ln}), compensator neutral current (i_{Cn}), dc bus voltages (v_{dc}) along with split capacitor voltages (v_{dc1}, v_{dc2}) and the amplitude of PCC voltage (V_S) are demonstrated under varying load conditions. It is observed that the amplitude of PCC voltage is regulated to the reference amplitude by the required reactive power compensation. The d_c bus voltages of two capacitors of the VSC of DSTATCOM are regulated to equal magnitude by the controller and the d_c bus voltage is maintained at the reference voltage under different load disturbances.

The dynamic performance of DSTATCOM with star/hexagon transformer for voltage regulation and harmonic elimination along with neutral current compensation is shown in Fig. 5. The PCC voltages (v_s), balanced supply currents (i_s), load currents (i_{La}, i_{Lb}, i_{Lc}), compensator currents (i_C), supply neutral current (i_{sn}), load neutral current (i_{Ln}), compensator neutral current (i_{Cn}), dc

bus voltage (v_{dc}) along with split capacitor voltages (v_{dc1}, v_{dc2}) and amplitude of PCC voltage (V_s) are demonstrated under varying loads. At 0.8 sec, the load is changed to two-phase load and to single-phase load at 0.9 sec. The loads are applied again at 1.0 sec. The PCC voltage is regulated to the reference amplitude value.

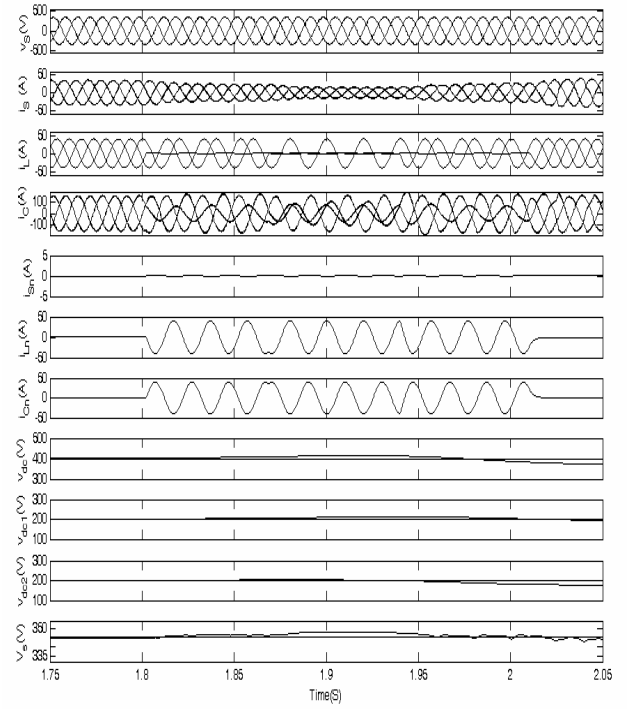

Fig. 4: Performance of proposed DSTATCOM for neutral current compensation, load balancing and voltage regulation.

The performance of the DSTATCOM system in the unity power factor (UPF) mode of operation is depicted in Fig. 6 and Fig. 7. The load balancing and neutral current compensation are demonstrated in Fig. 6 and the harmonic elimination, load balancing and neutral current compensation are demonstrated in Fig. 7. The PCC voltages (v_s), balanced sinusoidal supply currents (i_s), load currents (i_{La}, i_{Lb}, i_{Lc}), compensator currents (i_C), supply neutral current (i_{sn}), load neutral current (i_{Ln}), compensator neutral current (i_{Cn}), dc bus voltage (v_{dc}) along with split capacitor voltages (v_{dc1}, v_{dc2}) and amplitude of PCC voltage (V_s) are shown in both these cases. It is also observed that the PCC voltage is not regulated in both these cases as the compensator is operated in the UPF mode. The waveform of the load current and its harmonic spectrum is shown in Fig. 8 and the compensated supply current with its harmonic spectrum is shown in Fig. 9. The voltage at the PCC with its harmonic spectrum is shown in Fig. 10. It may be observed that the THD (total harmonic distortion) of the supply current is reduced less than 5% thus meeting the requirement of IEEE-519 standard [5].

V. CONCLUSION

The performance of a new topology of three-phase four-wire DSTATCOM consisting of the H-bridge VSC integrated to a star/hexagon transformer has been demonstrated for neutral current compensation along with reactive power compensation, harmonic elimination and load balancing. The star/hexagon transformer has mitigated the supply neutral current and it has been found effective for compensating the zero sequence fundamental and harmonics currents. The voltage regulation and power factor correction modes of operation of the DSTATCOM have been observed as expected ones. The dc bus voltage of the DSTATCOM has been regulated to the reference dc bus voltage under all varying loads. Moreover, an off the shelf two-leg, H-bridge VSC has been controlled for power quality compensation in the three-phase four-wire distribution system. The star/hexagon transformer configuration requires three single phase transformers and this provides isolation to the VSC along with power quality improvement and neutral current compensation.

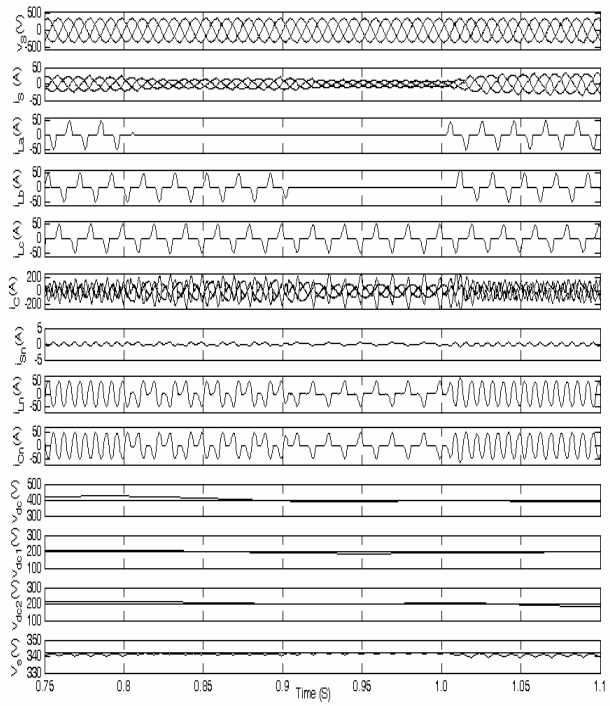

Fig. 5: Performance of proposed DSTATCOM for harmonic elimination, neutral current compensation, load balancing and voltage regulation.

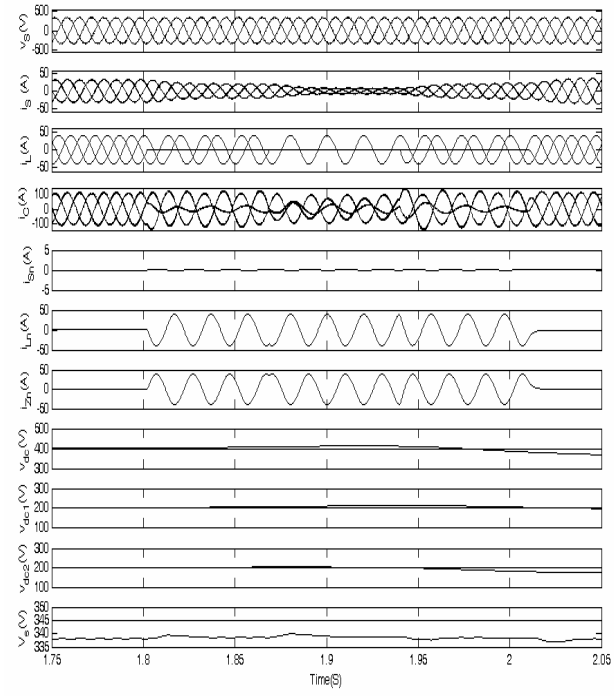

Fig. 6: Performance of proposed DSTATCOM for neutral current compensation, load balancing and power factor correction.

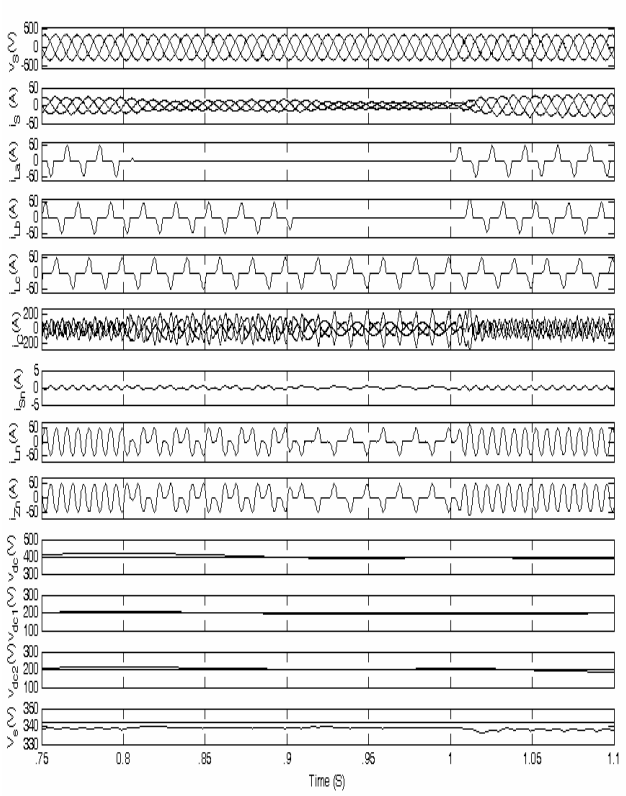

Fig. 7: Performance of proposed DSTATCOM for harmonic elimination, neutral current compensation, load balancing and power factor correction.

APPENDIX

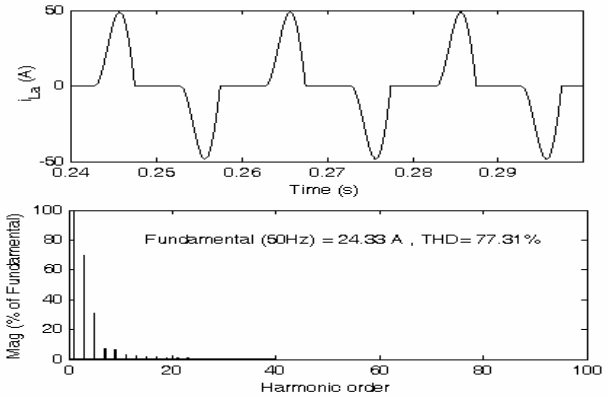

Fig. 8: Load voltage and harmonic spectrum

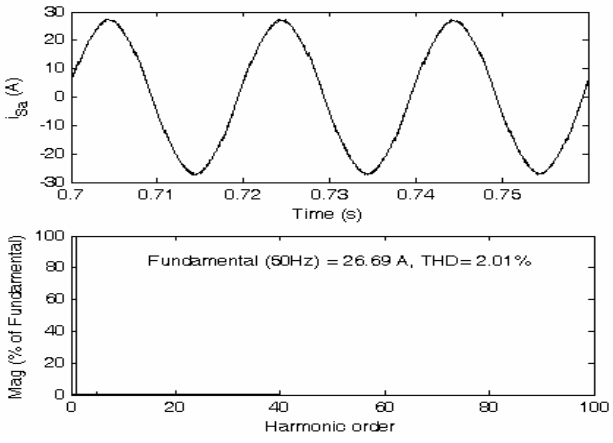

Fig. 9: Supply current and harmonic spectrum

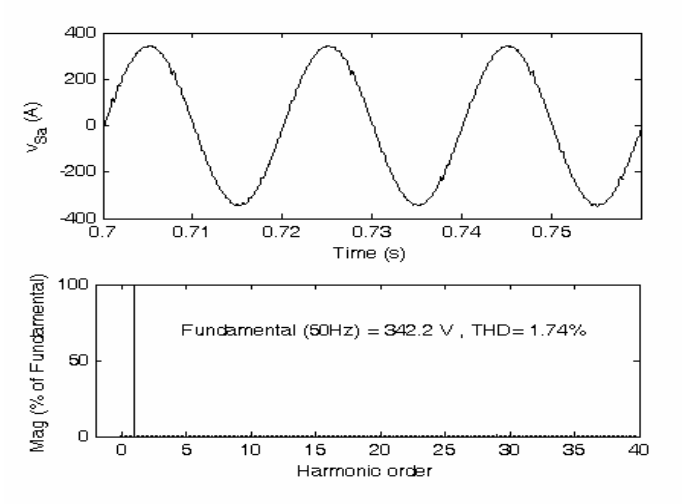

Fig. 10: PCC Voltage and harmonic spectrum

Line Impedance: R_s=0.01 Ω, L_s= 2 mH
Loads: (i) Linear: 20 kVA, 0.80 pf lag
(ii) Non-linear: Three single-phase bridge rectifiers with R = 25 Ω and C = 470 μF
Ripple filter: R_f= 5 Ω, C_f= 5 μF
DSTATCOM:
DC bus voltage of DSTATCOM: 400 V
Individual capacitor voltages: 200 V
DC bus capacitance of DSTATCOM:10000 μF
AC inductor: 4.2 mH
DC voltage PI controller: K_{pd}=0.19, K_{id}=6.25
DC equal bus voltages PI controller: K_p=0.09, K_i=2.5
PCC voltage PI controller: K_{pq} =0.9, K_{iq} =7.5
AC line voltage: 415V, 50 Hz
PWM switching frequency: 10 kHz
Star/Hexagon Transformer: Three 1-phase transformers of 5 kVA, 240V/120V/120V.

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BIOGRAPHIES

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H-Bridge VSC Based Voltage Controller for an Isolated Asynchronous Generator Supplying Three-Phase Four-Wire Loads

Gaurav Kumar Kasal[1] Bhim Singh[1]

Abstract – This paper presents a new configuration of a STATCOM based voltage controller for an isolated asynchronous generator (IAG) driven by bio-gas, diesel and gasoline engines and feeding 3-phase 4-wire consumer loads. The proposed controller consists of a two-leg IGBT (Insulated Gate Bipolar junction Transistor) based voltage source converter with an equal voltage distributed mid point capacitors at its DC link. The neutral point for the consumer loads is created using a tertiary winding zig-zag transformer. The tertiary winding allows the selection of the optimum voltage level of the DC link. The complete system is modeled and simulated using Simulink and PSB toolboxes. Extensive simulation results are presented to demonstrate the capability of the controller as a harmonic eliminator, a load balancer, alongwith as a voltage controller.

Keywords – Stand-alone power generation, two leg voltage source converter, mid point capacitors, voltage control, zig-zag transformer.

I. INTRODUCTION

Continuous depletion of fossil fuels and concern about the global warming, an importance of the locally available natural sources has increased such as hydro, biogas etc. In isolated applications for harnessing renewable energy from available non- conventional energy sources such hydro, and bio-mass, an asynchronous machine driven by a constant speed prime mover operated as an isolated asynchronous generator (IAG) with its excitation requirement being met by a capacitor bank connected across its terminals [1-3], has become the compatible option since last two decades. The increased emphasis on renewable energy sources has accelerated research and development of the IAG for autonomous power generation due to its simplicity, ruggedness and low cost. The fundamental problems with the IAG are its inability to control the terminal voltage under varying load conditions. Hence the limitations of an induction generator system with capacitor self excitation are poor voltage regulation, which results in under utilization of the machine. In order to regulate its terminal voltage with the load and to utilize the machine to its rated capacity an external source of the reactive current is required. A number of methods have been proposed in the literature for regulating the voltage of IAG for 3-phase 3-wire [3-5] constant speed, variable power applications. However here an attempt is made to investigate a voltage regulator for the 3-phase 4-wire loads on IAG in constant speed variable power isolated applications where consumer loads are distributed as single phase loads. Therefore, a need of 3-phase 4-wire system is essential and more effective than other configurations. In constant speed operation (prime mover such as diesel, gasoline and bio-mass engines) the drop in speed from no load to full load is almost negligible therefore variation in frequency is only because of slip which in turn depends on the amount of power required by the electrical loads. However, it needs the variable reactive power of the machine for regulating the voltage of IAG. Moreover, in such applications, the load balancing is also an essential requirement.

In this paper, a new configuration of the controller is proposed which is based on the two leg IGBT (Insulated Gate Bipolar Junction Transistor) based voltage source converter (VSC) with a mid point capacitors [6-8] at its DC bus. The neutral terminal for the loads is created using a zigzag transformer and its additional secondary windings. An advantage of a two leg voltage source converter is that number of IGBT switches are reduced compared to four leg VSC topology and compared to three single phase VSC with transformer topology and three leg VSC with mid point capacitors topology. In addition, the proposed novel voltage controller with an additional secondary winding in zig-zag transformer has facilitated the selection of suitable voltage rating of the DC bus capacitor and a zigzag transformer provides the path for the load neutral current [9,10]. The proposed voltage controller also functions as a harmonic eliminator and a load balancer [11].

II. SYSTEM CONFIGURATION

Fig. 1 shows a stand alone generating system along with the proposed voltage controller. The system consists of a constant speed prime mover (such as diesel, gasoline and biogas engines) driven squirrel cage asynchronous generator and its controller is connected at the point of common coupling through interfacing transformers. Two leg of the VSC are connected to the two phases while third phase is connected at the mid point of the DC bus capacitors. A zig-zag transformer is used to solve the problem of the neutral conductor and compared to other four wire topology system becomes less complex. The zig-zag transformer acts as a path for zero-sequence components of load currents while two leg VSC serves the purpose of harmonic elimination, load balancing and reactive power compensation. The zig-zag transformer consists of three tertiary winding transformers with the turn ratio of 2:2:1. Hence it is regarded as an open-circuit for the positive and negative sequence currents. The tertiary winding of the transformers facilitates to select the optimum voltage level of the DC bus capacitor.

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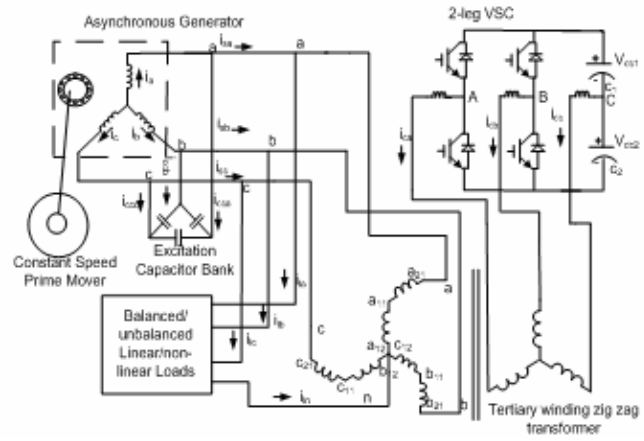


Fig. 1: Schematic diagram of a proposed system configuration.

III. Control Strategy

As shown in Fig. 2, the control strategy of the two leg voltage controller is realized through derivation of reference source currents (i^r_{sa}, i^r_{sb}). Reference source currents consist of two components one is in phase or active power component (i^r_{da}, i^r_{db}) for the self supporting DC bus of VSC while other one is in quadrature or reactive power component (i^r_{qa}, i^r_{qb}) for regulating the terminal voltage. The amplitude of active power component of the source current (I_{dm}) is estimated using two PI controllers among which, one is used to control the voltage of DC bus of VSC while another one is used for equal voltage distribution across the DC bus capacitors. The output of the first PI controller is estimated by comparing the reference DC bus voltage (V_{dcref}) with the sensed DC bus voltage (V_{dc}). The output of the second PI controller is estimated by comparing the voltages across both capacitors (V_{dc1}) and (V_{dc2}) and error signal is optimized using a second PI controller. The sum of output of both PI controllers (I_{dm1}) and (I_{dm2}) gives the active power current component (I_{dm}) of the reference source current. The multiplication of I_{dm} with in-phase unit amplitude templates (u_{ad}, u_{bd}) yields the in-phase component of instantaneous reference source currents. These (u_{ad}, u_{bd}) templates are sinusoidal functions, which are derived by unit templates of in phase with line voltages (u_{ab}, u_{bc}, u_{ca}). These templates (u_{ab}, u_{bc}, u_{ca}) are derived by dividing the AC voltages v_{ab}, v_{bc} and v_{ca} by their amplitude V_t. To generate the quadrature component of reference source currents, another set of sinusoidal quadrature unity amplitude templates (u_{aq}, u_{bq}, u_{cq}) is obtained from in-phase unit templates (u_{abd}, u_{bcd}, u_{cad}). The multiplication of these components (u_{aq}, u_{bq}) with output of the PI (Proportional-Integral) AC voltage controller (I_{qm}) gives the quadrature, or reactive power component of reference source currents. The sum of instantaneous quadrature and in-phase component of source currents is the reference source currents (i^r_{sa}, i^r_{sb}), and each phase source current is compared with the corresponding reference source current to generate the PWM switching signals for VSC of the controller.

IV. Control Algorithm

Basic equations of the control scheme of the proposed controller are as follows.

Different components of the controller used in an asynchronous generator-system shown in Fig. 1, are modeled as follows**.** Three line voltages at the generator terminals (v_{ab}, v_{bc} and v_{ca}) are considered sinusoidal and hence their amplitude is computed as

$$V_t = \sqrt{(2/3)}\ (v_{ab}^2 + v_{bc}^2 + v_{ca}^2) \quad (1)$$

The unit template in phase with v_{ab}, v_{bc} and v_{ca} are derived as

$$u_{ab} = v_{ab}/V_t;\ u_{bc} = v_{bc}/V_t;\ u_{ca} = v_{ca}/V_t \quad (2)$$

From these in phase line voltage templates, unit templates in phase with phase voltage can be estimated as:

$$u_{ad} = (\sqrt{3/2})\ u_{abd} + \{1/(2\sqrt{3})\}\ \{(u_{bcd} - u_{cad})\} \quad (3)$$

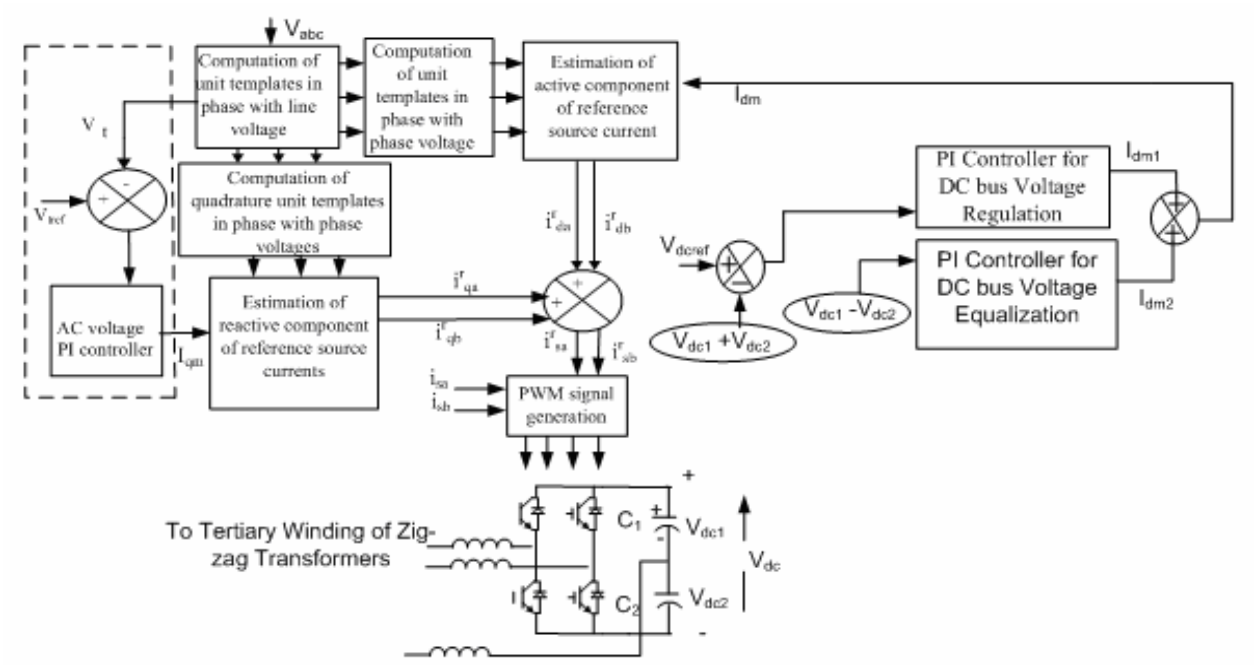


Fig. 2: Control scheme of the proposed controller.

$$u_{bd} = -(\sqrt{3}/2)\, u_{abd} + \{(1/(2\sqrt{3}))\}\{(u_{bcd}-u_{cad})\} \quad (4)$$

$$u_{cd} = -(1/\sqrt{3})\{(u_{bcd}-u_{cad})\} \quad (5)$$

and templates in quadrature with phase voltages are

$$u_{aq} = (1/2)\, u_{abd} - \sqrt{3}\,(u_{bcd} - u_{cad}) / (2\sqrt{3}) \quad (6)$$

$$u_{bq} = (1/2)\, u_{abd} + \sqrt{3}\,(u_{bcd} - u_{cad}) / (2\sqrt{3}) \quad (7)$$

$$u_{cq} = - u_{abd} \quad (8)$$

A. In-Phase Component of Reference Source Currents

The error in DC bus voltage of STATCOM ($V_{dcer(n)}$) at n^{th} sampling instant is:

$$V_{dcer(n)} = V_{dcref(n)} - V_{dc(n)} \quad (9)$$

where $V_{dcref(n)}$ is the reference DC voltage and $V_{dc(n)}$ is the sensed DC link voltage of the VSC. The output of the DC bus PI controller (I_{dm1}) for maintaining DC bus voltage of the VSC at the n^{th} sampling instant is expressed as:

$$I_{dm1(n)} = I_{dm1(n-1)} + K_{pd1}\{V_{dcer1(n)} - V_{dcer1(n-1)}\} + K_{id1} V_{dcer1(n)} \quad (10)$$

K_{pd1} and K_{id1} are the proportional and integral gain constants of the PI controller.

Then second part of active component of reference source current (I_{dm2}) is calculated for equal voltage distribution across the mid-point capacitor as.

$$V_{dcer(n)} = V_{dc1(n)} - V_{dc2(n)} \quad (11)$$

where $V_{dc1(n)}$ and $V_{dc1(n)}$ are the voltage across the capacitors C_1 and C_2 .

The output of the PI controller ($I_{dm2(n)}$) for maintaining equal capacitors voltages at the n^{th} sampling instant is expressed as

$$I_{dm2(n)} = I_{dm2(n-1)} + K_{pd2}\{V_{dcer2(n)} - V_{dcer2(n-1)}\} + K_{id2} V_{dcer2(n)} \quad (12)$$

Total active component (I_{dm}) of reference source current is estimated as:

$$I_{dm} = I_{dm1} + I_{dm2} \quad (13)$$

Instantaneous values of in-phase components of reference source currents are estimated as:

$$i^{r}_{da} = I_{dm}\, u_{ad}; \quad i^{r}_{db} = I_{dm}\, u_{bd} \quad (14)$$

B. Computation of Reactive Component of Reference Source Current

The AC voltage error V_{er} at the n^{th} sampling instant as

$$V_{er(n)} = V_{tmref(n)} - V_{tm(n)} \quad (15)$$

where $V_{tmref(n)}$ is the amplitude of reference AC terminal voltage and $V_{tm(n)}$ is the amplitude of the sensed three-phase AC voltage at the terminals of an asynchronous generator at n^{th} instant.

The output of the PI controller ($I_{qm(n)}$) for maintaining constant AC terminal voltage at the n^{th} sampling instant is expressed as

$$I_{qm(n)} = I_{qm(n-1)} + K_{pa}\{V_{er(n)} - V_{er(n-1)}\} + K_{ia} V_{er(n)} \quad (16)$$

where K_{pa} and K_{ia} are the proportional and integral gain constants of the proportional integral (PI) controller (values are given in Appendix). $V_{er\,(n)}$ and $V_{er(n-1)}$ are the voltage errors in n^{th} and $(n-1)^{th}$ instant and $I_{qm(n-1)}$ is the amplitude of quadrature component of the reference source current at $(n-1)^{th}$ instant.

The instantaneous quadrature components of reference source currents are estimated as

$$i^{r}_{qa} = I_{qm}\, u_{aq}; \quad i^{r}_{qb} = I_{qm}\, u_{bq}; \quad (17)$$

C. Computation of Reference Source Current

The reference source currents are sum of in-phase and quadrature components of the reference source currents as

$$i^{r}_{sa} = i^{r}_{qa} + i^{r}_{da} \quad (18)$$

$$i^{r}_{sb} = i^{r}_{qb} + i^{r}_{db} \quad (19)$$

D. PWM Signal Generation

Reference source currents (i^{r}_{sa}, i^{r}_{sb} and i^{r}_{sc}) are compared with sensed source currents (i_{sa}, i_{sb} and i_{sc}). The current errors are computed as

$$i_{saerr} = i^{r}_{sa} - i_{sa} \quad (20)$$

$$i_{sberr} = i^{r}_{sb} - i_{sb} \quad (21)$$

These current errors are amplified and amplified signals are compared with fixed frequency triangular wave to generate the gating signals to the IGBTs and similar logic is applied to generate the gating signals for other phase of VSC.

V. MATLAB Based Modeling

The proposed controller is modeled and simulated in MATLAB using Simulink and PSB (Power System Block set) toolboxes. A 7.5 kW, 415V, 50Hz asynchronous machine is used as a generator including the saturation characteristics of the machine, which is determined by synchronous speed test [5]. A delta connected excitation capacitor is used to generate the rated voltage at no-load [5], while an additional demand of the reactive power of the generator during load variation is met by the proposed controller. An in-built universal bridge is used as a two leg voltage source converter. The tertiary winding zig –zag transformer is modeled using transformer blocks. All necessary equations to model the control algorithm such as calculation of terminal voltage, unit vectors etc. are carried out using function blocks. Simulation is carried out in MATLAB version of 7.3 using ode (23tb/stiff/TR-BDF-2) solver in discrete mode at 5e-6 step size.

VI. Results and Discussion

Figs. 3-5 show the performance of the proposed standalone generating system under the dynamic conditions of varying loads. These figures show the performance of the controller for supplying balanced/ unbalanced, linear/ non-linear loads respectively. Fig. 5 demonstrates the waveforms and the total harmonic distortion (THD) of the generator voltage, generator current and load current under the non-linear load condition and it is observed that in all conditions, the controller responds in desirable manner. Simulated transient waveforms of the generator voltage (v_{abc}), generator current (i_{abc}), capacitor current (i_{cca}), load currents (i_{labc}), controller current (i_{cabc}), load neutral current (i_{ln}), terminal voltage (V_t), DC link voltage (V_{dc}) and voltage across both the capacitors (V_{dc1} and V_{dc2}), are given in different dynamic conditions.

A. Performance of the Controller for Feeding 3-Phase 4-Wire 0.8pf Lagging Linear Loads

Fig. 3 demonstrates the controller performance for isolated asynchronous generator for feeding 3-phase 4-wire loads. At 2.5 s, when 0.8pf lagging balanced reactive load of

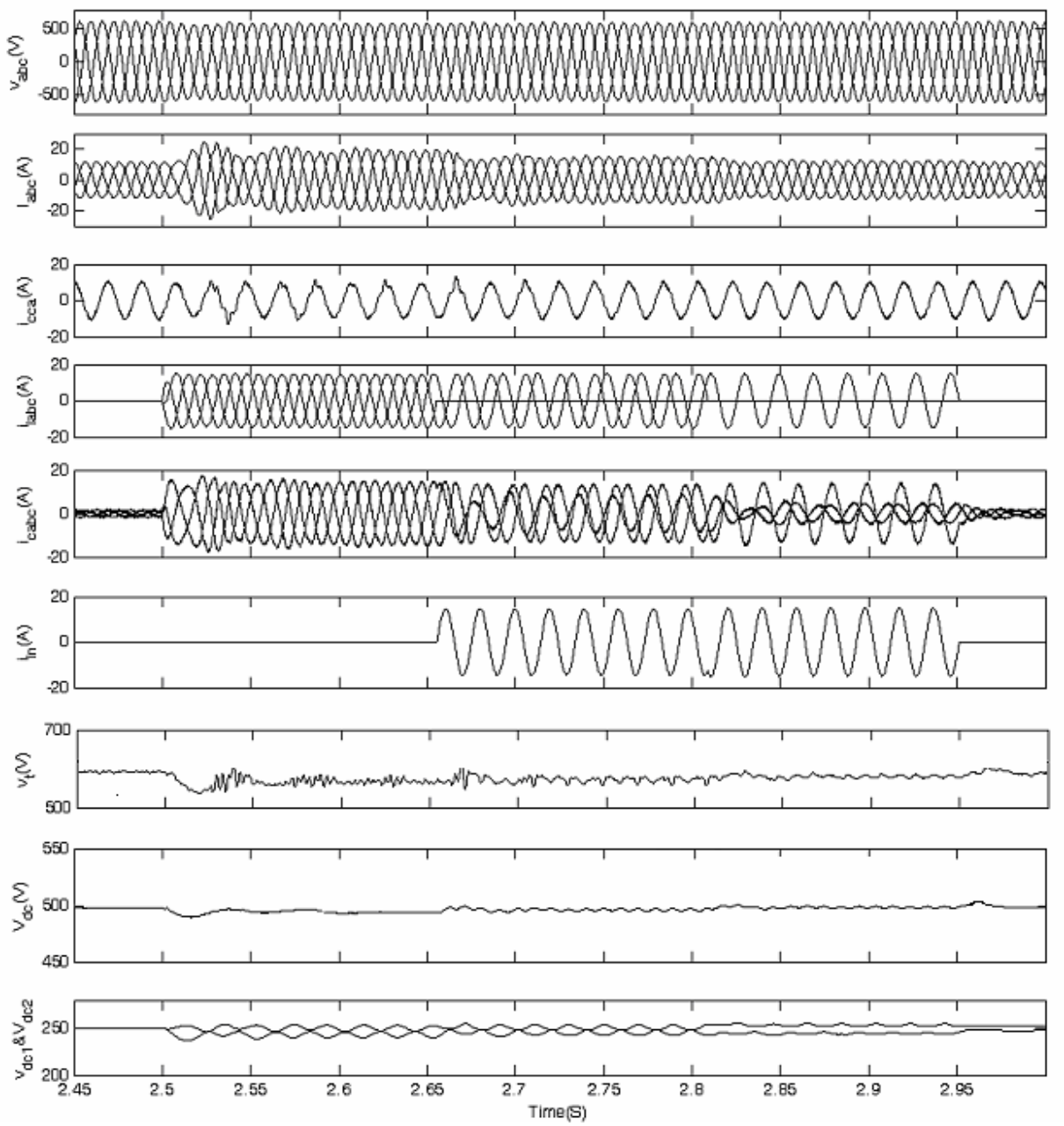


Fig. 3: Performance of the controller under the condition of feeding varying 3-Phase 4-wire 0.8 pf lagging reactive loads

around 6kW is applied at PCC, the compensator is supplying the reactive current to regulate the voltage at its reference value. At 2.65 s, one phase and later on at 2.8 s, other phase of the load is opened, the load becomes unbalanced, which is compensated by the controller as shown in Fig. 3.

A. Performance of the Controller for Feeding 3-Phase 4-Wire Non-linear Loads

In the similar manner, Fig. 4 demonstrates the performance of the controller for isolated asynchronous generators feeding 3-phase 4-wire non-linear loads. At 2.5s, on the application single-phase diode bridge rectifier based 6kW three non-linear loads between each phase and neutral, the voltage is regulated by the controller. At 2.7 s, one phase and later on at 2.9 s, other phase is opened, the load becomes unbalanced on the system while on the generator side source currents remain balanced which demonstrates the load balancing aspects of the controller.

B. Power Quality Aspects

Harmonic spectrum and waveform of the generator voltage, current and the load current are demonstrated in Fig. 5 under balanced conditions of non-linear loads. Under the condition of balanced load currents having THD (total harmonic distortion) of the order of 79.05%, these are compensated by the controller and THD of the voltage and currents of the generator is observed around 1.78% and 2.71% respectively. The THD of generated voltage and generator current is obtained less than 5% and it meets the requirements of IEEE -519 standard [12]. Hence from these results, it is demonstrated that along with voltage regulation, load balancing, and harmonic elimination are achieved using the proposed controller.

VII. CONCLUSION

A novel reduced switch configuration of a voltage controller has been investigated for a stand alone power generating system along with tertiary winding zigzag

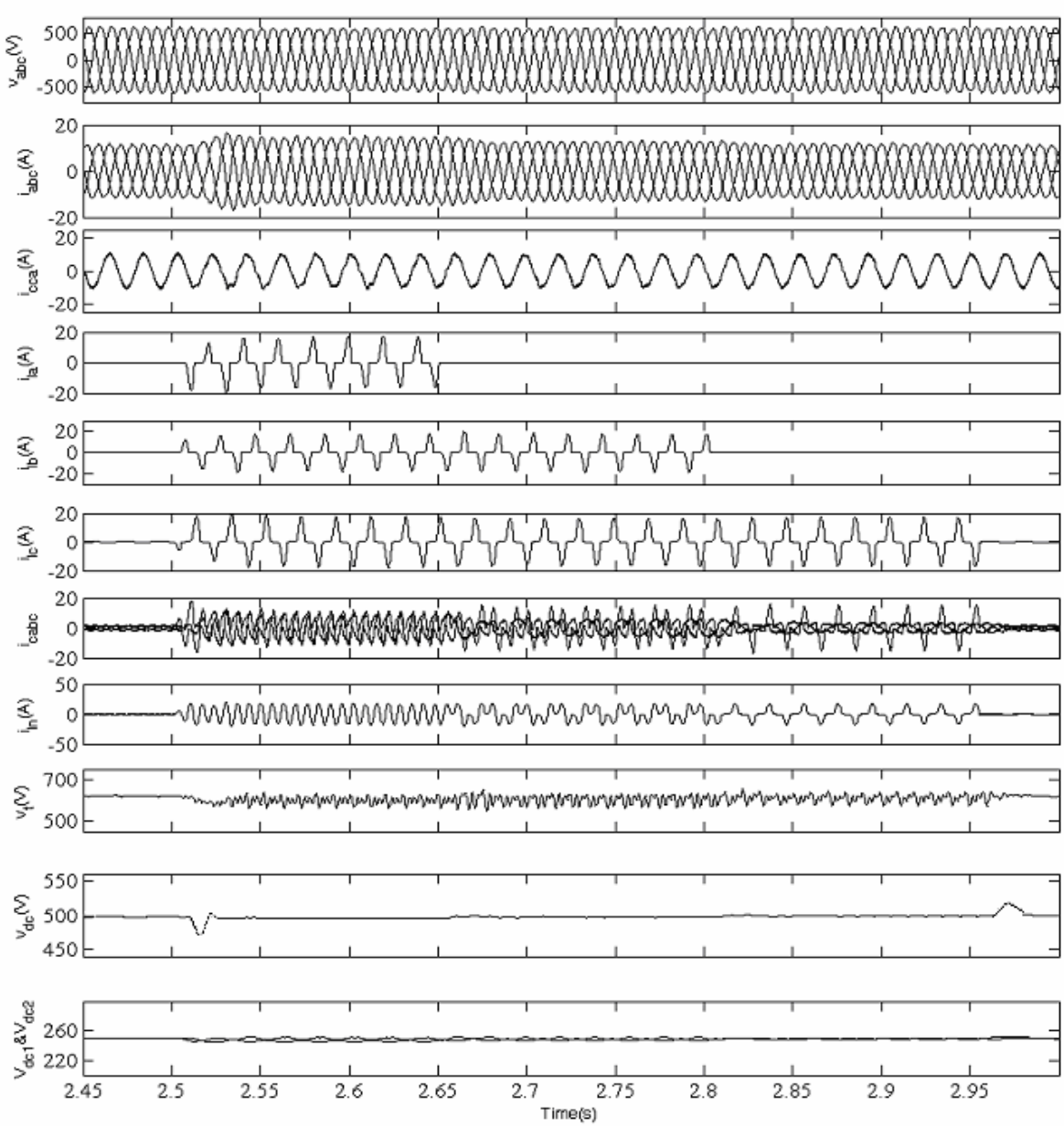


Fig. 4: Performance of the controller at varying 3-Phase 4-wire non-linear loads.

transformer. The size, cost and complexity of the controller have comparatively reduced in comparision to other 3-phase 4-wire topology of the VSC based voltage controller in a stand alone power generation. The simulation results have demonstrated the capability of the controller as a harmonic eliminator, a load balancer along with voltage regulator in a stand-alone power generating system. The performance of the controller has been demonstrated under different dynamic conditions such as varying consumer loads and it has been observed that the proposed controller has given quite satisfactory performance of IAG system.

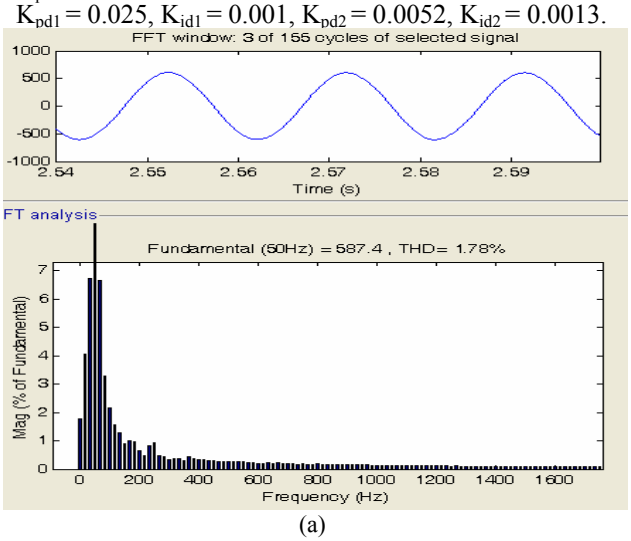
VIII. Appendix

A. *The parameters of 7.5kW, 415V, 50Hz, Y-Connected, 4-Pole asynchronous machine are given below.*

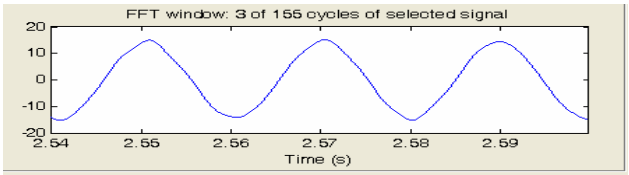
$R_s = 1\ \Omega$, $R_r = 0.77\Omega$, $X_{lr} = X_{ls} = 1.5\Omega$, $J = 0.1384 kg\text{-}m^2$
$L_m = 0.134H$ ($I_m < 3.16A$)
$L_m = 9e\text{-}5I_m^2 - 0.0087I_m + 0.1643$ ($3.16 < I_m < 12.72$)
$L_m = 0.068H$ ($I_m > 12.72A$).

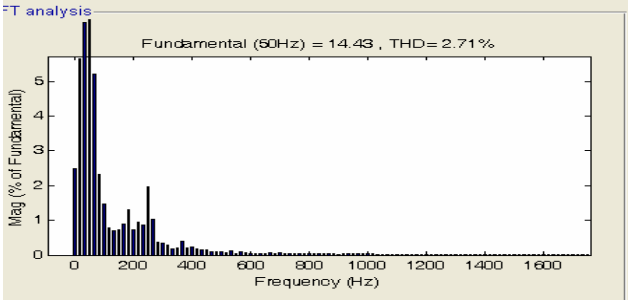
B. *Controller Parameters*

$L_f = 4mH$, $R_f = 0.1\Omega$, and $C_{dc} = 4000\ \mu F$.
$K_{pa} = 0.14$, $K_{ia} = 0.0015$.
$K_{pd1} = 0.025$, $K_{id1} = 0.001$, $K_{pd2} = 0.0052$, $K_{id2} = 0.0013$.



(a)





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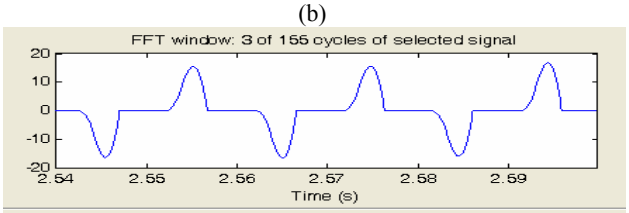

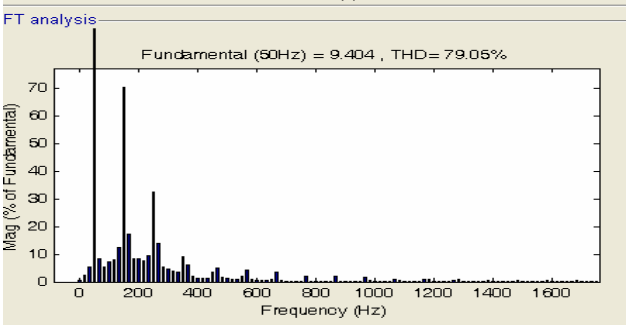

(c)

Fig. 5: Waveforms and harmonic spectra of generator voltage (v_a), generator current (i_a) and consumer load current (i_{lc}) feeding balanced non-linear load.

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Harmonics Elimination in Multilevel Inverter with Two Unequal Voltage Batteries

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Abstract – Elimination of harmonics in a multilevel inverter with two unequal dc sources is considered. That is, for a given fundamental output voltage, our aim is to find the switching angles, that produce the fundamental while not generating specifically chosen harmonics. A procedure is given to find all sets of switching angles for which the fundamental is produced while lower order harmonics are eliminated. This is done by first converting the transcendental equations that specify the elimination of the harmonics into an equivalent set of polynomial equations. Then, using the mathematical theory of resultants, solution to this equivalent problem is found.

Keywords – Multilevel inverter, harmonics elimination, unequal voltage batteries

I. Introduction

Multilevel inverters provide more than two voltage levels. A desired output voltage waveform can be synthesized from the multiple voltage levels with less distortion, at low switching frequency, higher efficiency, and lower voltage rating devices. An important issue in designing an effective multilevel inverter is to ensure that, the total harmonic distortion (THD) in the output voltage waveform is small [4]. This requires an (mathematical) algorithm to determine when the switching should be done so as not to produce harmonics and a fast real-time computing system to implement the strategy. A method was reported in [2] and [3] that presented a procedure the switching angles for the H-bridges in a cascaded converter using the mathematical theory of resultants. In that work, a complete solution was presented for computing all possible switching angles that achieved the requisite fundamental voltage and eliminated lower order harmonics. However, it was assumed that the dc sources were all equal, which will probably not be the case in applications even if the sources are nominally unequal. Here, it is shown how the method in [3] can be extended to two un-equal dc source inverter. Specifically, eliminating harmonics in a multilevel converter in which the separate dc sources do not have equal voltage levels is considered. Generally each phase of a cascaded multilevel converter requires n DC sources for 2n + 1 levels. For many applications, to get many separate DC sources is difficult, and too many DC sources will require many long cables and could lead to voltage unbalance among the DC sources. To reduce the number of DC sources required when the cascaded H-bridge multilevel converter is applied to a motor drive, a scheme is proposed in [1] that allows the use of two unequal DC sources to generate 7 level equal step multilevel inverter output instead of three equal batteries.

This scheme provides the capability to produce higher voltages (where they are needed) at low switching frequency, has inherent low switching losses and high conversion efficiency. For electric/hybrid electric vehicle motor drive applications, two H-bridges for each phase is a good tradeoff between performance and cost.

For the required fundamental output voltage, it is desired to find out the switching times (angles) that produce the fundamental and no specifically defined harmonics. In this paper, the lower order harmonics are eliminated making use of two unequal DC voltages for H-bridges.

II. Cascaded H-Bridges

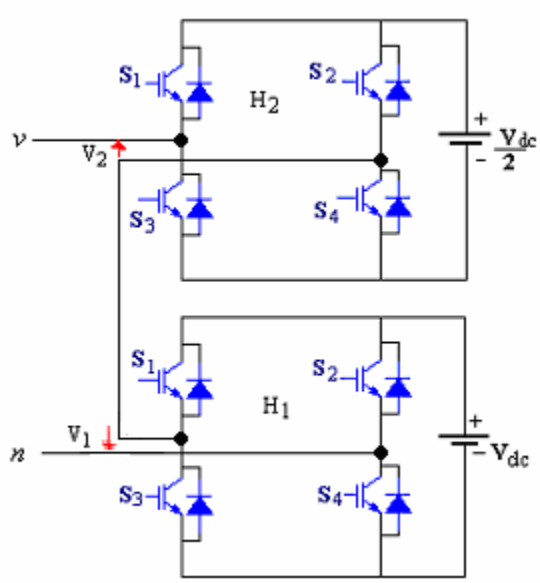

Fig. 1: Single phase multilevel cascaded H-bridge inverter.

The cascaded multilevel inverter consists of a series of H-bridge inverter units. As previously mentioned, the general purpose of this multilevel inverter is to synthesize a desired voltage from several separate dc sources (SDCSs), like batteries, fuel cells, solar cells, and ultra-capacitors. Fig. 1 shows a single-phase structure of a cascade inverter with SDCSs [6]. Each SDCS is connected to a single-phase full-bridge inverter. Each inverter level can generate three different voltage outputs, $+V_{DC}$, 0, $-V_{DC}$ with different combinations of the four switches, S_1, S_2, S_3, and S_4.

The conventional method of generating 7 level multilevel inverter output waveform is, by using three batteries of equal magnitude and three cascaded H-bridges. In this scheme the duty cycle for each of the voltage level is

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different. If this pattern of duty cycle is used on a motor drive continuously, the level 1 battery is cycled on for a much longer duration than the level 3 battery. This means that the level 1 battery will discharge much more than the level 3 battery.

To operate a cascaded multilevel inverter using two unequal DC source, we have proposed to use the first DC sources (i.e., the battery connected to first H-bridge, H_1) as V_{dc} and the magnitude of voltage of second battery as $\frac{V_{dc}}{2}$.Fig. 1 shows cascaded H-bridges multilevel inverter with two unequal batteries. The DC source for the first H-bridge (H_1) is a battery or fuel cell V_1 with an output voltage of V_{dc}, and the DC source for the second H-bridge (H_2) is V_2 with an output voltage of $\frac{V_{dc}}{2}$. The output voltage of the cascaded multilevel inverter is

$$V(t) = v_1(t) + v_2(t) \quad . \qquad (1)$$

By applying the triggering pulses to the switches of H_1 appropriately, the output voltage V_1 can be made equal to V_{dC}, 0, or -V_{dC}. while the output voltage of H_2 i.e., V_2 can be made equal to $\frac{V_{dc}}{2}$, 0, or -$\frac{V_{dc}}{2}$. by applying the triggering pulses to the switches of H_2 appropriately.

The 7 output voltages of the inverter are $\left(\frac{V_{dc}}{2}+V_{dc}\right)$, , , $\left(\frac{V_{dc}}{2}\right)$, 0, $-\left(\frac{V_{dc}}{2}\right)$, $-V_{dc}$, $-\left(\frac{V_{dc}}{2}+v_{dc}\right)$ which are 7 possible output levels. Fig. 2 shows the 7 level equal step output voltage waveform,

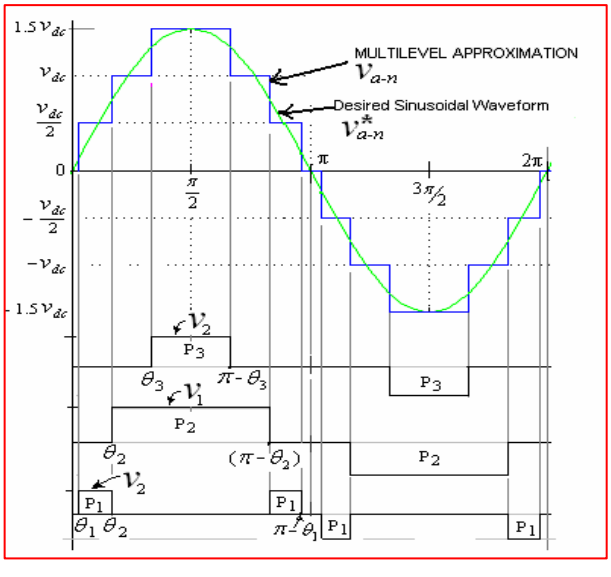

Fig. 2: Seven level equal step output voltage

This problem does not occur for the switching scheme shown above. In this paper a switching scheme is proposed in which v_1=output of H_1 =V_{dc} and v_2=output of H_2 = $V_{dc}/2$ From θ_1 to θ_2, voltage v_2 will appear at the output (i.e. $V_{a\text{-}n}$) and from θ_2 to θ_3, voltage v_1 will appear, from θ_3 to $\theta_{\pi-\theta3}$ voltages (v_1+v_2) will appear, from $\theta_{\pi-\theta3}$ to $\theta_{\pi-\theta2}$ voltage v_1 will appear, and from $\theta_{\pi-\theta2}$ to $\theta_{\pi-\theta1}$ voltage v_2 will appear at the out put. Hence both the batteries discharge equally in every half cycle (i.e. for every 90^0).

III. Switching Algorithm for Multilevel Inverter

The Fourier series expansion of the 7-level equal step output voltage waveform is [4]

$$\left.\begin{aligned} V(\omega t) = \sum_{n=1,3,5\ldots}^{\infty} \frac{4V_{dc}}{n\pi}(\cos n\theta_1) \\ +(\cos n\theta_2)+(\cos n\theta_3)\sin(n\omega t) \end{aligned}\right\} \qquad (2)$$

where 'n' is the harmonic number of the output voltage. Given a desired fundamental voltage V_1, one wants to determine the switching angles θ_1, θ_2, θ_3 so that $V(\omega t) = V_1 \sin(\omega t)$, and specific higher order harmonics are eliminated [8]-[10]. For three-phase motor drive applications, the triplen harmonics in each phase need not be considered as they automatically disappear in the line-to-line voltages. In this paper, the goal is to eliminate the 5th harmonic and the 7th harmonic can be filtered out. Mathematically, this can be formulated as the solution to the following equations:

$$\left.\begin{aligned} \cos\theta_1 + \cos\theta_2 + \cos\theta_3 = m \\ \cos 5\theta_1 + \cos 5\theta_2 + \cos 5\theta_3 = 0 \\ \cos 7\theta_1 + \cos 7\theta_2 + \cos 7\theta_3 = 0 \end{aligned}\right\} \qquad (3)$$

This is a system of three transcendental equations with three unknowns θ_1, θ_2, and θ_3. There are many ways to solve for the angles. One approach to solving this set of nonlinear transcendental equations (3) is to use an iterative method such as the Newton–Raphson method [4]. In this work, the method given in is extended to find *all* solutions to (3). This methodology is based on the mathematical theory of resultants of polynomials which is a systematic procedure for finding the roots of *polynomial* equations. In this method, the set of equations (3) is converted to a polynomial system shown below by setting $x_1 = \cos\theta_1$, $x_2 = \cos\theta_2$, $x_3 = \cos\theta_3$ and using the trigonometric identities

$$\cos 5\theta = 5\cos\theta - 20\cos^3\theta + 16\cos^5\theta$$
$$\cos(7\theta) = -7\cos\theta + 56\cos^3\theta - 112\cos^5\theta + 64\cos^7\theta$$

to transform (3) into the equivalent conditions

$$\left.\begin{aligned} p_1(x) \triangleq \mathrm{V}_1 x_1 + V_2 x_2 + V_3 x_3 - m = 0 \\ p_5(x) \triangleq \sum_{i=1}^{3} \mathrm{V}_i\left(5x_i - 20x_i^{\,3} + 16x_i^{\,5}\right) = 0 \\ p_7(x) \triangleq \sum_{i=1}^{3} \mathrm{V}_i\left(-7x_i - 56x_i^{\,3} + 112x_i^{\,5} + 64x_i^{\,7}\right) = 0 \end{aligned}\right\} \qquad (4)$$

Where $x = (x_1, x_2, x_3)$ and $m \triangleq \mathrm{V}_f/(4V_{dc}/\pi)$. The modulation index is $m_a = \frac{m}{n} = V_f/(n4V_{dc}/\pi)$. This follows from the fact that each inverter has a dc source that is nominally equal to V_{dc} so that the maximum output voltage of the multilevel inverter is nV_{dc}. Consequently, a square wave of amplitude nV_{dc} results in the maximum fundamental output possible of $V_{f\max} = 4nV_{dc}/\pi$ so that

$$m_a \triangleq V_f/V_{f\max} = V_f/(n4V_{dc}/\pi) = m/n$$

This is now a set of three *polynomial* equations in the three unknowns x_1, x_2, x_3. Further, the solutions must satisfy $0 \le x_3 < x_2 < x_1 \le 1$ [4].

substituting $x_3 = \dfrac{(m-(V_1x_1+V_2x_2))}{V_3}$ into P_5, P_7 leads to,

$$P_5(x_1,x_2) = V_1(5x_1 - 20x_1^3 + 16x_1^5) + V_2(5x_2 - 20x_2^2 + 16x_2^5) + 5V_3\left(\frac{m-(V_1x_1+V_2x_2)}{V_3}\right) - 20V_3\left(\frac{m-(V_1x_1+V_2x_2)}{V_3}\right)^3 + 16V_3\left(\frac{m-(V_1x_1+V_2x_2)}{V_3}\right)^5 \quad (5)$$

and

$$P_7(x_1,x_2) = V_1(-7x_1 + 56x_1^3 - 112x_1^5 + 64x_1^7) + V_2(-7x_2 + 56x_2^3 112x_2^5 + 64x_2^7) - 7V_3\left(\frac{m-(V_1x_1+V_2x_2)}{V_3}\right) + 56V_3\left(\frac{m-(V_1x_1+V_2x_2)}{V_3}\right)^3 - 112V_3\left(\frac{m-(V_1x_1+V_2x_2)}{V_3}\right)^5 + 64V_3\left(\frac{m-(V_1x_1+V_2x_2)}{V_3}\right)^7. \quad (6)$$

IV. Elimination using Resultants

In order to explain how one computes the zero sets of polynomial systems, utilizes *elimination theory* and uses the notion of *resultants*. Briefly, one considers $a(x_1,x_2)$ and $b(x_1,x_2)$ as polynomials in x_2 whose coefficients are polynomials in x_1 [4]. Then, for example, letting $a(x_1,x_2)$ and $b(x_1,x_2)$ have degrees 3 and 2, respectively in x_2, they may be written in the form

$$a(x_1,x_2) = a_3(x_1)x_2^3 + a_2(x_1)x_2^2 + a_1(x_1)x_2 + a_0(x_1) \quad (7)$$

$$b(x_1,x_2) = b_2(x_1)a_2^2 + b_1(x_1)x_2 + b_0(x_1) \quad (8)$$

The $(n \times n)$ *Sylvester* matrix,

where $n = \deg_{x_2}\{a(x_1,x_2)\} + \deg_{x_2}\{b(x_1,x_2)\} = 2+3 = 5$ is defined by,

$$S_{a,b}(x_1) = \begin{bmatrix} a_0(x_1) & 0 & b_0(x_1) & 0 & 0 \\ a_1(x_1) & a_0(x_1) & b_1(x_1) & b_0(x_1) & 0 \\ a_2(x_1) & a_1(x_1) & b_2(x_1) & b_1(x_1) & b_0(x_1) \\ a_3(x_1) & a_2(x_1) & 0 & b_2(x_1) & b_1(x_1) \\ 0 & a_3(x_1) & 0 & 0 & b_2(x_1) \end{bmatrix} \quad (9)$$

The *resultant* polynomial is then defined by,

$$r_1(x_1) = \mathrm{Res}\,(a(x_1,x_2), b(x_1,x_2), x_2) \triangleq \det S_{a,b}(x_1) \quad (10)$$

and is the result of solving $a(x_1,x_2)=0$ and $b(x_1,x_2)=0$ simultaneously for x_1, i.e., eliminating x_2. This can be referred in [12] – [15] for an explanation of this fact. The computational challenge for this approach is in the symbolic calculation of the determinant of the Sylvester matrix. However, the results in [16], [17] show that this computation can be carried out quite efficiently.

V. Experimental Results

To validate the proposed cascaded H-bridge multilevel motor drive control scheme, a three-phase cascaded H-bridge multilevel inverter has been developed. The switches used for this inverter are the IGBTs GT60M303 (Toshiba Make). The gating pulses are generated by microcontroller board. A 3-phase induction motor is selected with the specifications shown in the table-1 below. Also motor model is developed using MATLAB Simulink.

Table 1: Specifications of the motor

S. No.	Type of the motor	3-ϕ Induction motor
1	Rated output power	3700 watts (5 HP)
2	Rated line-to-line voltage	415 volts
3	Rated current	8.4 amps
4	Number of poles	4
5	Frequency of the supply voltage	50 Hz
6	Rated speed	1485 rpm
7	Type of winding	Y-connected

The parameters of this motor are calculated by conducting No-load test, Blocked Rotor test and Retardation test. This motor model is simulated using MATLAB and the simulated results are compared with that of practical results. It is found that these two results are very close to each other. Then the motor model is simulated with the proposed cascaded multilevel inverter.

Table 2: Results of motor on load test, at rated voltage 415V

S. No.	I_L Amps	W_{in} Watts	T_L N-m	N rpm	I/p Watts	O/p Watts	η %
1	4.5	200	0	1480	200	0	0
2	4.9	900	2.53	1463	900	387.6	43
3	5.5	1600	7.6	1413	1600	1124.5	70.2
4	6.1	2100	10.96	1376	2100	1579	75.2
5	6.8	3100	15.18	1320	3100	2098	67.6

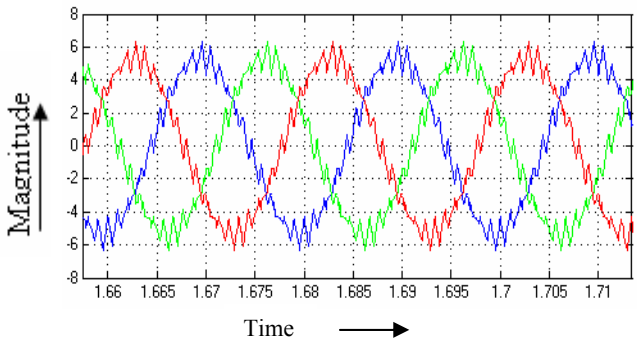

Fig. 3: Stator current, motor fed from SPWM Inverter

Fig. 3 shows the stator currents of three phase induction motor on no-load fed from 2 level inverter. In this fig. even though the waveform looks close to sinusoidal, it has distortion. Fig. 4 is the stator currents of the same motor fed with 7 level inverter. Fig 5 shows the spectrum. It is

observed that the distortion is almost reduced. Hence the motor runs smoothly and safely. Fig. 6 is the three phase output voltage of multilevel (7 Level) inverter with two unequal voltages.

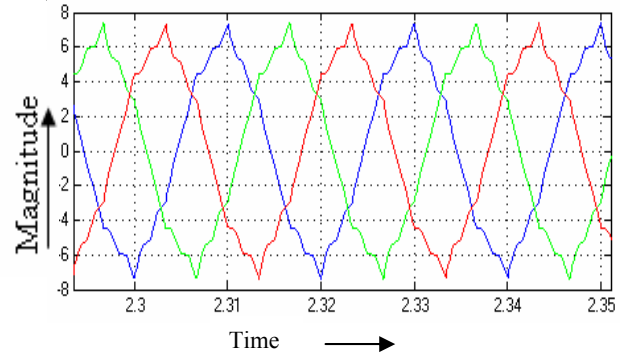

Fig.4: Stator current, motor fed from ML Inverter

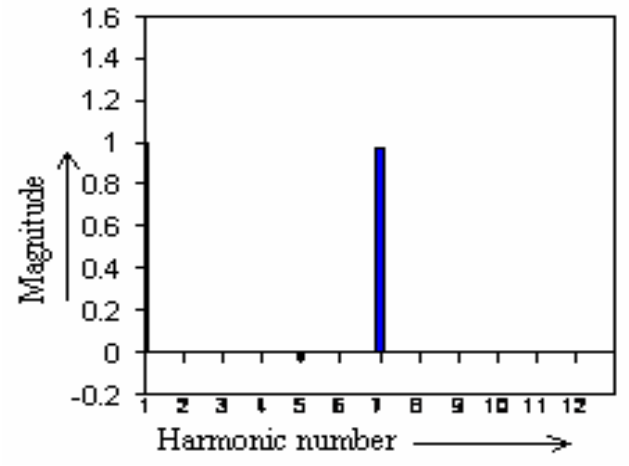

Fig. 5: Harmonic spectrum of Line-to-Line Vg

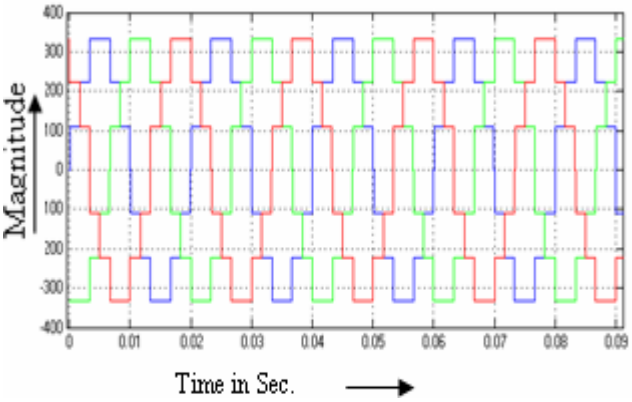

Fig. 6: Output voltage waveform of MLI (3 phase)

IV. Conclusion

Elimination theory and the notion of resultants can be used to eliminate the lower order harmonics in a multilevel inverter that has unequal dc sources. This method is expected to have widespread application as most multilevel converters do not have dc sources that are equal. Also as the number of batteries are reduced, the Electrical Vehicle mileage will also be improved. Both the batteries discharge equally in every half cycle (i.e. for every 90^0). By looking into harmonic spectrum, we observe that, all the lower order harmonics are eliminated, only the magnitude of 7^{th} harmonic, whose frequency is very high (350Hz) compared to fundamental frequency (50Hz). Hence it can be easily filtered out using a filter capacitor.

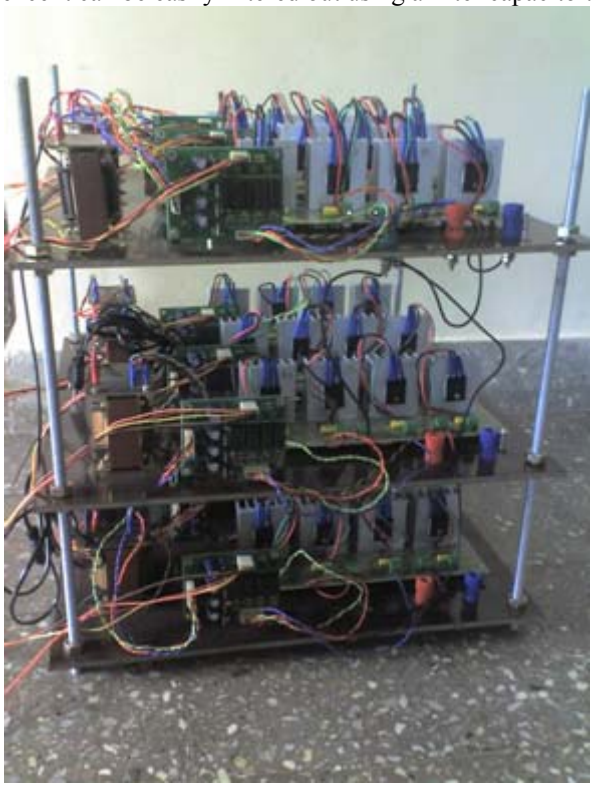

Fig. 7: Photograph of experimental setup

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Implementation of Novel Low Cost Multilevel DC-Link Inverter with Harmonic Profile Improvement

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Abstract – Harmonics is one of the most important criteria that decide the performance of the electrical devices. To reduce the harmonics, filters are used in inverter but it increases the cost and size of inverters. The multilevel inverters (MLI) are very interesting solution as it reduces harmonics and has the characteristics of synthesizing an approximate sinusoidal voltage on several DC levels. The significant advantages of multilevel configuration are voltage sharing both statically and dynamically and it produces better voltage waveforms with less harmonic contents. One particular disadvantage is it increases greater number of power semiconductor switches. To overcome this disadvantage a multilevel DC link inverter (MLDCL) is discussed in this paper. This comparatively reduces the number of switches, their gate drivers, compared with the existing MLI counterparts with harmonic profile improvement. Optimization of switching angle is performed using Simulated Annealing (SA) to reduce the 5 th, 7 th and 9th order harmonics and it is applied to a seven level cascaded MLDCL. The hardware is implemented using microcontroller based on the optimized firing angle obtained using SA.

Keywords - Multilevel inverter, optimized harmonic elimination, simulated annealing, THD

I. INTRODUCTION

The multilevel voltage source inverters are recently applied in many industrial applications such as ac power supplies, static VAR compensators, drive systems, and distributed energy resources (DER) area. Especially in DER area, because several batteries, fuel cells, solar cells, or rectified wind turbines or micro turbine can be connected through a multilevel inverter to feed a load or interconnected to the ac grid without voltage balancing problem [1]. In addition, multilevel inverters have a lower switching frequency than the standard PWM inverters and thus reduce the switching losses. The significant advantages of multilevel configuration are the harmonic reduction in the output waveform without increasing switching frequency or decreasing the inverter power output [2]. It also ensure even voltage sharing, both statically and dynamically.

Multilevel inverter synthesizes a desired voltage from several levels of dc voltages with low harmonics. As the number of levels increases, the harmonic distortion of the output wave decreases [5]. But the disadvantage is increase in number of switches and their gate drivers.

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As the number of level increases, the harmonic distortion of the output wave decreases. For reducing harmonics, if PWM or space vector modulation is used, it gives complexity in switching frequency in operation. Another approach is to find the switching angles in order to eliminate the specified harmonics. The mathematical theory of resultant is used to compute optimum switching angle [3]-[5]. But the disadvantage is complexity in solving polynomial equations. By employing optimized harmonic stepped waveform technique along with the multilevel topology, a low Total Harmonic Distortion (THD) output waveform without any filter circuit is possible [6]-[8]. A new Multilevel inverter topology using an H-bridge output stage with a bi-directional auxiliary switch is discussed [9].On the other hand, because of the low on state resistance and fast switching capabilities MOSFET's are utilized in multilevel inverters to reduce the cost or to provide a high bandwidth output voltage at high efficiency [10] –[11].

This paper presents a new topology of Multi Level DC Link Inverter (MLDCL), based on a MLDCL and a bridge inverter and it reduces the number of power semiconductor switches and gate drivers as the number of voltage level increases. The MLDCL's can be diode clamped, capacitor clamped or cascaded H Bridge inverter. The cascaded MLDCL topology is discussed in this paper. The MLDCL's provides a dc voltage with the shape of a staircase approximating the rectified shape of a commanded sinusoidal wave to the bridge inverter, which in turn alternates the polarity to produce an ac voltage. For a given number of voltage levels m, the required number of active switches is $2*(m-1)$ for the existing multilevel inverters but is $m+3$ for the MLDCL inverters [12]. Simulated Annealing (SA) based optimization technique is applied to determine the switching angle for cascaded MLDCL inverter, which eliminates specified higher order harmonics while maintaining the required fundamental voltage.

II. CASCADED MULTILEVEL INVERTER

A. Cascaded H-Bridge Multilevel Inverter

The traditional cascaded inverter formed by connecting single phase H-Bridge or cells in series as shown in Fig. 1. Each cell supplied by separate dc source and generates output voltage with different duty ratio. In this paper a seven level-cascaded multilevel inverter is considered and the switching angles θ_1, θ_2, θ_3 are obtained for harmonic optimization. The number of voltage levels generated by using N number of DC sources is given by $2N+1$. The ac terminal voltages of different level inverters are connected in series. By different combinations of the four switches, s1-s4, each inverter level can generate three differentvoltage outputs, $+Vdc$, $-Vdc$, and zero. The ac

outputs of each of the different level of full-bridge inverters are connected in series such that the synthesized voltage waveform is the sum of the inverter outputs.

B. Cascaded Half-Bridge–Based MLDCL Inverter

The cascaded MLDCL inverter consists of half bridge cells and one full bridge cell. Each half-bridge cell has two switches S_1 and S_2. They operate in a toggle fashion. The cell source is bypassed when S_1 is on and S_2 is off. The cell source adds to the DC link voltage when S_1 is off and S_2 is on. The half bridge cell produces DC bus voltage waveform with the shape of staircase and the full bridge inverter cell alternates the voltage polarity to produce an AC voltage of staircase waveform. A seven level MLDCL inverter is considered in this paper and it is shown in Fig. 2. Single-phase bridge inverter contains four switches from S_a to S_d. They are always work in pairs at the fundamental frequency of the output voltage. Specifically, the MLDCL formed by the n half-bridge cells provides a staircase-shaped dc-bus voltage of n steps to the full bridge inverter, which in turn alternates the voltage polarity to produce an ac voltage V_{an} of a staircase shape with $(2*n+1)$ levels .The IGBT is used for switches S_a, S_b, S_c, S_d of full bridge inverter as the voltage rating is higher.

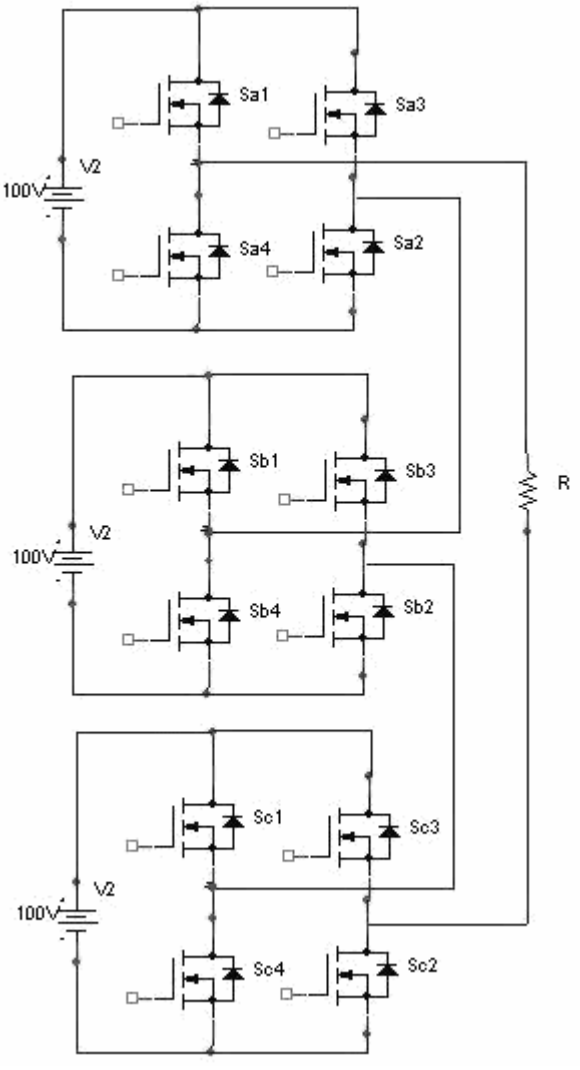

Fig. 1: Traditional 7-level cascaded multilevel inverter

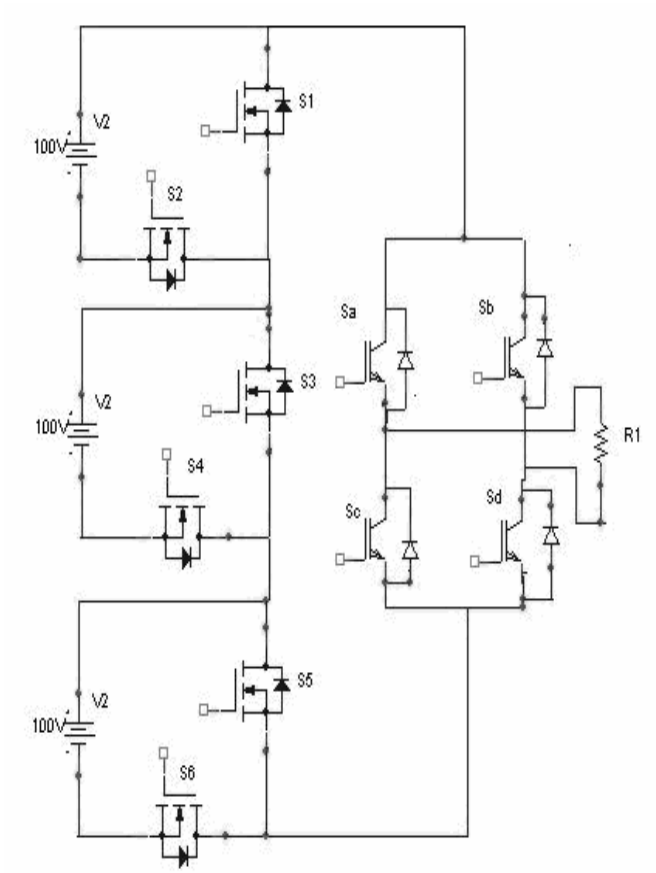

Fig. 2: 7-level Cascaded multilevel DC link inverter

C. Optimization using Simulated Annealing

Optimized harmonic stepped waveform technique is used to optimize the switching angles. 2_s+1 output levels can be synthesized with H-bridge inverters and separate dc sources (SDCSs). It consists of 3 switching angles θ_1, θ_2, θ_3 in each cycle as shown in Fig. 3. These voltage levels are supplied by SDCSs, whose amplitudes may be different or same. By considering the waveform, there are three possible optimization techniques to reduce the voltage THD. 1) step heights are optimized with equally spaced steps. 2) step spaces are optimized with the steps of equal height; and 3) optimizing both heights and spaces. This paper focuses on the second method, which uses equal voltage amplitude and optimizes the switching angles. By employing optimized harmonic stepped waveform technique along with the multilevel topology, a low Total Harmonic Distortion (THD) output waveform without any filter circuit is possible. By using above technique the energy function is obtained and solved using SA.

Simulated Annealing (SA) is a randomized algorithm for solving the global optimization problem. In the fields of chemistry and physics, there is a technique called Annealing used to create solid state metallic by slowly cooling the melted metal. The energy function E is the function to be minimized. The temperature T decreases gradually during the process. D is the difference between the energies of two states E_new and E_current. The Probability function depends on T and *D.* i.e.

exp (– (D/T))

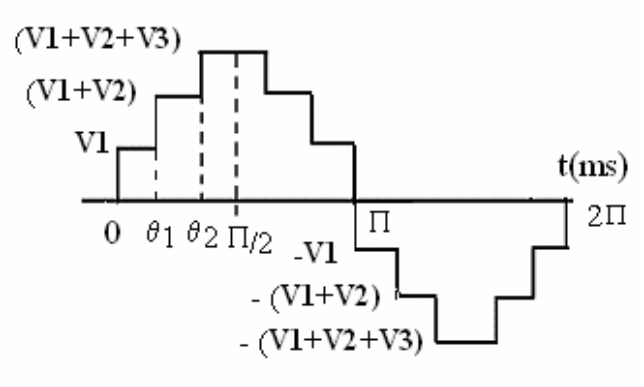

Fig. 3: The quarter-wave symmetric multilevel waveform

The idea of iterative improvement algorithms is to begin with a potential solution and to make adjustments to the solution over much iteration, moving the solution gradually toward a global optimum. In this project, the energy function is the total Harmonic distortion (THD) and is given in the equation (2). Higher number of iteration and temperature increase the rate of convergence.

$$THD = \frac{\sqrt{\sum_{n=2}^{200} 1/n \left[\sum_{k=1}^{N} (-1)^{k+1} \cos n\alpha_k\right]}}{\sum_{k=1}^{N} (-1)^{k+1} \cos n\alpha_k} \qquad (2)$$

N is the number of switching angles per quarter
n is the harmonic order
α_k is the calculated switching angles.

The steps for formulating a problem and applying SA as follows:

- Initialize temperature to 2000, iteration
- Select switching angles, current E, at random
- Substitute in Energy function
- Update E Generated
- While Temp>1
- For 1 to iteration
- Select new angles, in the neighborhood of current angles using the two Interchange methods with random values
- Update angles Generated
- Update E Generated
- Calculate D= *E*_new – *E*_current
  If (D<=0)
  Best E= *E*_new
  Else if random [0, 1] < exp – (D/T)
  Best E = *E*_new
  End if.
- Iteration = iteration-1
- End iteration.
- Temp =Temp -1
- End

This Simulated Annealing code is programmed in the MATLAB m-file. This code can find the switching angle solutions for a multilevel inverter with any number of levels and for the elimination of any number of harmonics.

III. Simulation And Experimental Results

A. Simulation results

Simulated Annealing is used to determine the optimum switching angles and the results are shown in table I. The simulated waveform of MLDCL inverter without optimization is given in the Fig. 4. The simulated waveform of MLDCL inverter by using the optimized angle from simulated annealing is given in the Fig. 5. The simulation is performed with 100V DC source using IGBT and MOSFET. Ode23tb solver with relative tolerance is used for simulation. Harmonic spectrum is obtained using power GUI in Simulink.

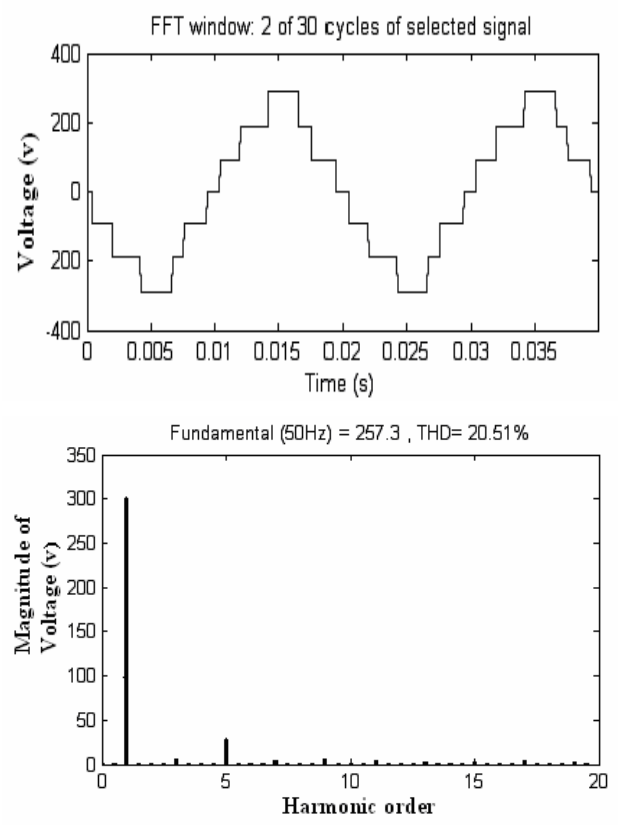

Fig. 4: Simulated waveforms and harmonic spectrum of seven level cascaded MLDCL inverter without optimization

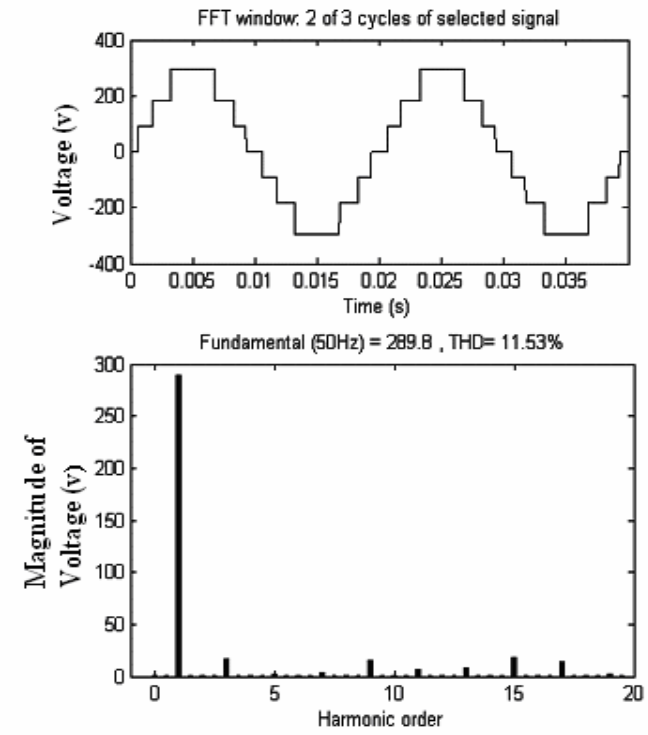

Fig. 5: Simulated waveforms and harmonic spectrum of seven level cascaded MLDCL inverter using SA.

B. Comparison of multilevel dc-link inverter and existing counterparts

The multilevel dc-link inverter effectively reduce the number of switches and their gate drivers. Cascaded multilevel inverter requires $2*$ (m-1) number of switches and the cascaded MLDCL require only (m+3) number of switches. In addition, the new multilevel dc-link inverter saves the cost of the inverter circuit by having an additional module of single-phase full bridge (SPFB) inverter. With higher voltage levels, only two switches are enough for fabricating each bridge in multilevel dc-link (MLDCL) with four switches in SPFB inverter.

Fig. 6 mentions the reduction in number of switches when increasing the number of levels. As the number of level increases switches are considerably reduced. For a eleven level inverter cascaded Multilevel inverter requires 20 switches and cascaded MLDCL requires 14 switches.

Table 1: component count comparison—seven levels

No of switches for seven level(m=7)		Optimised angles			THD (%)
Multilevel DC link(m+3)	Multilevel 2*(m-1)	θ_1	θ_2	θ_3	11.53
10	12	9.57	36.9	54.2	

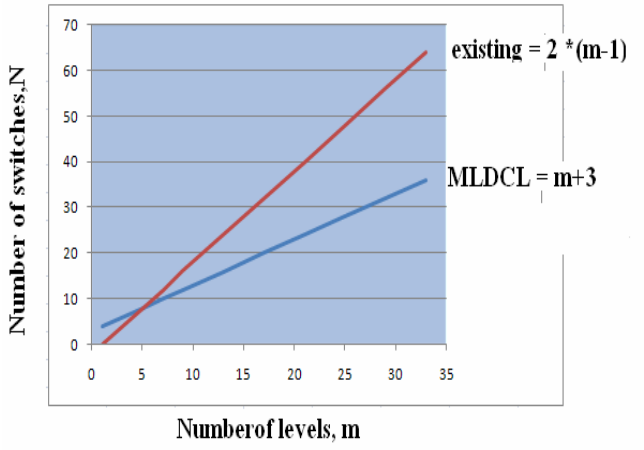

Fig. 6: Comparison of required number of switches.

C. Hardware implementation

A microcontroller based seven level-cascaded multilevel dc-link inverter is fabricated and tested. The circuit diagram of opto-isolator with half bridge cell and the experimental setup is given in Fig. 7 and Fig. 8 respectively. The microcontroller PIC 16F877A is used to generate the pulses. Port c of the microcontroller generates pulse for triggering the MOSFET. Timer 0 is used for producing the delay required for the duration T_{ON} and T_{OFF}. The microcontroller operates at a clock frequency of 20 MHz. The opto-isolator 4N35 is used for isolation between the controller and the inverter circuit. The experimental parameters are given in Table 2. The pulses are generated based on the optimized firing angles obtained by SA method in simulation. The hardware prototype is shown in Fig. 9. The oscillogram of voltage waveform is given in Fig. 10.

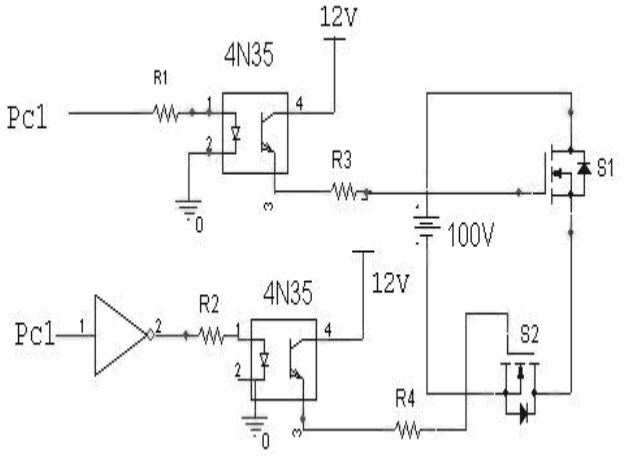

Fig. 7: Circuit diagram of opto coupler and half bridge cell

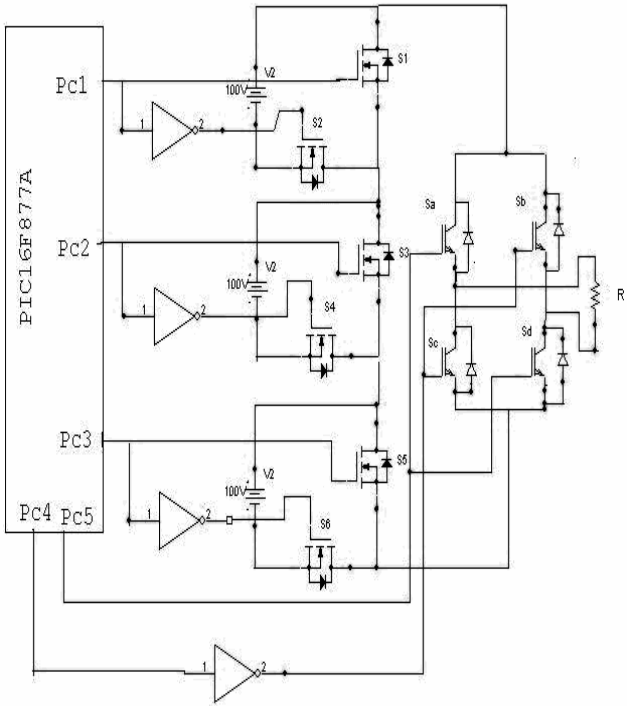

Fig. 8: Experimental circuit diagram

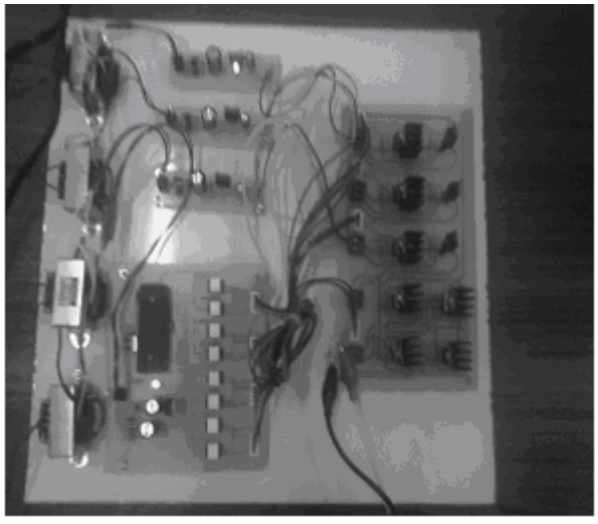

Fig. 9: Hardware prototype

Table 2: Experimental parameters

Components	Value
MOSFET	IRF740
PIC Microcontroller	PIC16F877A
IGBT	CM400DY
Optocoupler	4N35
DC Voltage	100V
R-Load	50Ω

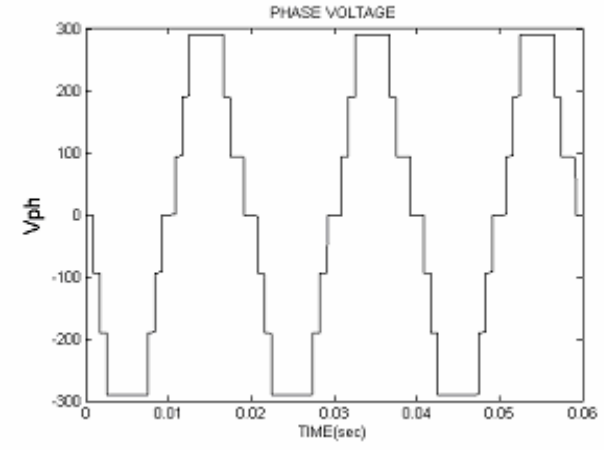

Fig. 10: Oscillogram of voltage waveform

IV. Conclusion

Cascaded multilevel dc-link, inverter is simulated using MATLAB Simulink based on the optimized firing angle obtained from SA and the convergence time is 180 seconds. The hardware prototype is implemented using Microcontroller. A seven level-cascaded multilevel dc-link inverter is successfully fabricated and tested. The Total Harmonic Distortion obtained using simulation is 11.53% and hardware is 13.21%. The optimized angle obtained by simulation is used for experimental verification and it shows harmonic profile improvement .The new multilevel dc-link inverter needs least number of components than the existing multilevel inverters for the same level of output waveform. By increasing the number of levels of the multilevel dc-link inverter topologies, the parameters like switches, gate driver, are reduced with better output waveform.

Acknowledgment

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A Hybrid Seven- Level Inverter for Fuel Cell Power Conditioning System

R. Seyezhai [1] B.L. Mathur [2]

Abstract –This paper investigates the potentials of a hybrid cascaded seven-level inverter for fuel cell power conditioning systems (PCS). Fuel cell is one of the most important sources of distributed energy because of its high efficiency, high energy density, plus high reliability and long life due to few moving parts. This article proposes a suitable modulation strategy for the hybrid inverter that fulfills the required performance specifications of a fuel cell power system. The main advantage of this topology is that the modulation, control and protection requirements of each bridge are modular and it requires only a single dc source in each phase leg. Among the several modulation strategies proposed for the seven- level inverter, the space vector modulation (SVM) and carrier based PWM are the most popular ones. And this paper focuses on the Phase Disposition (PD) carrier PWM method as it gives less harmonic distortion on the line to line output. The PDPWM is implemented using an FPGA processor so that better resolution is achieved in the control of multilevel inverter output voltage magnitude and it is verified experimentally.

Keywords – Hybrid multilevel inverter, fuel cell, multicarrier PWM, PCS

I. INTRODUCTION

Multilevel inverters are used to synthesize a desired single or three-phase voltage waveform. They are of special interest in the distributed energy sources area because several batteries, fuel cell, solar cell and wind turbine can be connected through multilevel inverter to feed a load without voltage balance problems. There are several topologies of multilevel inverter but the one considered in this paper is the hybrid cascaded multilevel inverter (HCMLI). This topology has many advantages not only in terms of its simple structure but also allows the use of a single dc source as the first dc source with the remaining (n-1) dc sources being capacitors[1]. The voltage regulation of the capacitor is the key issue and this is achieved by the switching state redundancy of the proposed modulation strategy. This scheme also provides the ability to produce higher voltages at higher speeds with low switching losses and high conversion efficiency. For the cascaded multilevel inverter variety of modulation strategies have been reported, with the most popular being carrier – based and space vector modulation (SVM). Several multi carrier techniques have been developed to reduce the distortion in multilevel inverter, based on the classical SPWM with triangular carriers. Multicarrier PWM methods can be categorized into two groups: Carrier Disposition methods (CD), where the reference waveform is sampled through a number of carrier waveforms displaced by continuous increments of the reference waveform amplitude and phase shifted (PS) PWM methods, through a number of carrier waveforms displaced by continuous increments of the reference waveform amplitude and phase shifted (PS) PWM methods, where multiple carriers are phase shifted accordingly [2]. This paper focuses on the Phase disposition (PD) carrier PWM method as it gives a least THD of 5.2%. Both the HCMLI circuit topology and its control scheme are described in detail and their performance is verified based on simulation and experimental results.

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II. HYBRID CASCADED SEVEN-LEVEL INVERTER

A hybrid seven- level cascaded H-bridge inverter has two H-bridges for each phase. One H-bridge is connected to a dc source and another is connected to a capacitor, as shown in Fig. 1. The dc source for the first H-bridge (H_1) could be a battery or fuel cell with an output voltage of V_{dc}, and the dc source for the second H-bridge (H_2) is the capacitor voltage, to be held at V_c. The output voltage of the first H-bridge is denoted by V_1, and the output of the second H-bridge is denoted by V_2 so that the output voltage of the cascaded multilevel converter is V (t) = V_1 (t) +V_2 (t).

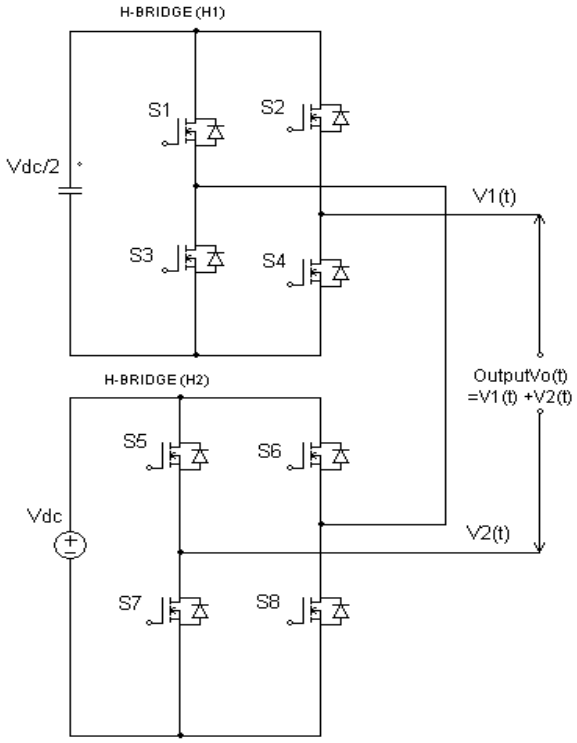

Fig. 1: Hybrid cascaded multilevel inverter

By opening and closing the switches of H_1 appropriately, the output voltage V_1 can be made equal to -V_{dc}, *0*, or +V_{dc} while the output voltage of H_2 can be made equal to –V_c, *0*, or V_c.(refer Fig. 2.). Therefore, the output voltage of the converter is a combination of V_{dc} and V_c which can have nine possible values -(V_{dc} +Vc), -(V_{dc}-V_c),-V_c, *0*, V_c, (V_{dc}-

V_c), V_{dc}, (V_{dc}+V_c) and -Vdc. For the nine possible levels used in a cycle, -(V_{dc}-V_c) and (V_{dc}-V_c) can be used to charge the capacitors; -(V_{dc}+V_c),-V_c, V_c and (V_{dc}+V_c) can be used can be used to discharge the capacitors.

The advantages of Hybrid topology are:

- Reduced number of dc sources.
- High speed capability
- Low output switching frequency
- Low switching loss
- High conversion efficiency.
- Flexibility to enhance.

The table I given below shows the comparison of topologies for multilevel inverter. Here the number of switches and number of dc sources required for the different topologies for producing the same seven - level output are compared. The hybrid multilevel inverter topology shows the least number of switches and the least number of dc sources and its output voltage waveform is shown in Fig. 2.

Table I: Comparison of topologies for multilevel inverter

Topology	Primary Devices	DC Buses/ Capacitors	Levels in the Output
Diode Clamped	36	6	7
Flying Capacitor	36	16	7
Conventional H-Bridge	36	9	7
Hybrid H-Bridge	24	6	7

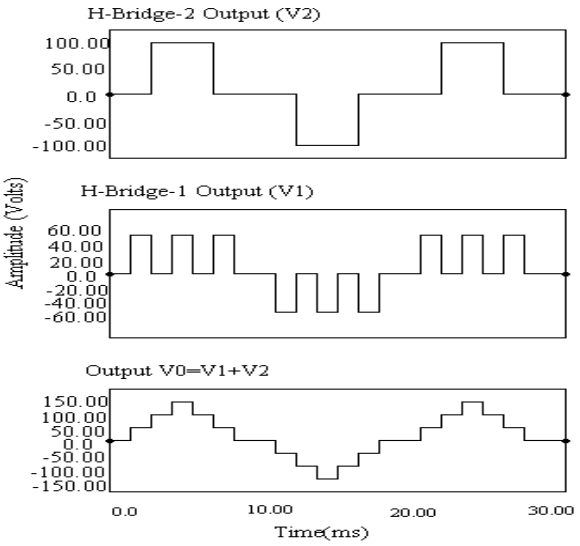

Fig. 2: Output voltage waveform of hybrid cascaded seven level inverter.

III. Proposed Control Scheme for the Hybrid Seven-Level Inverter

There are many control techniques used in multilevel inverters and the most popular being carrier – based and space vector modulation (SVM). Several multi carrier techniques have been developed to reduce the distortion in multilevel inverter, based on the classical SPWM with triangular carriers, Multicarrier PWM methods can be categorized into two groups: Carrier Disposition methods (CD), where the reference waveform is sampled through a number of carrier waveforms displaced by continuous increments of the reference waveform amplitude and phase shifted (PS) PWM methods, where multiple carriers are phase shifted accordingly [3]. The carrier disposition method comprises phase opposition disposition (POD) method, phase disposition (PD) method and Alternative phase opposition disposition (APOD) method. This paper focuses on the Phase disposition (PD) carrier PWM method as it gives a least THD of 5.2%. The PDPWM is implemented using Spartan FPGA processor so that better resolution is achieved.

A. Phase Disposition Modulation Method (PDPWM)

In this method carriers are the same in frequency, amplitude and phases, but they are just different in dc offset to occupy contiguous bands as shown in Fig. 3. For this technique, significant harmonic energy is concentrated at the carrier frequency f_c, but because it is a co-phase component, it does not appear in the line voltage. It should be noted that the other harmonic components are centered on the carrier frequency as sidebands. Among the discussed techniques, PD technique has less harmonic distortion on line voltages [4]. An example of the carriers that is used in a two modular seven- level PWM inverter is shown in Fig.3.There are six distinct carriers, all in phase with one another and with the same magnitudes(A_c), the difference between the carriers is that they are all displaced by dc offset. The reference waveform has peak-to-peak amplitude A_m, a frequency f_m, and its zero is centered in the middle of the carrier set. The reference is continuously compared with each of the carrier signals. If the reference is greater than a carrier signal, then the active device corresponding to that carrier is switched on; and if the reference is less than a carrier signal, then the active device corresponding to that carrier is switched off [5]. With reference to Fig. 1. if we consider the first bridge H_1, the modulation rules are:

If $V_{ref} > V_{triangle\text{-}1}$, then the switch S_1 – on, S_3- off.

If $V_{ref} < V_{triangle\text{-}1}$, then the switch S_1 –off, S_3 - on.

The resultant gate control is obtained by comparing each of the carriers to the related part of the sinusoidal reference, which in turn controls a specific gate and the switching pattern for PDPWM is shown in Fig. 4.

In multicarrier PWM, the amplitude modulation index m_a, and the frequency ratio m_f, is defined as

$$m_a = \frac{A_m}{(m-1).A_c} \quad (1)$$

$$m_f = \frac{f_c}{f_m} \quad (2)$$

when applying this method to a multi- modular system the carriers are divided amongst each of the modules. Therefore in the case of obtaining a seven- level output voltage from a two- modular PWM hex bridge inverter, the top module is responsible for producing the bottom of the positive level, and the bottom module is responsible for the top PWM level. The Phase Disposition method has significant harmonic energy and is concentrated at the

carrier frequency, which is usually set at a moderate to high value [6].

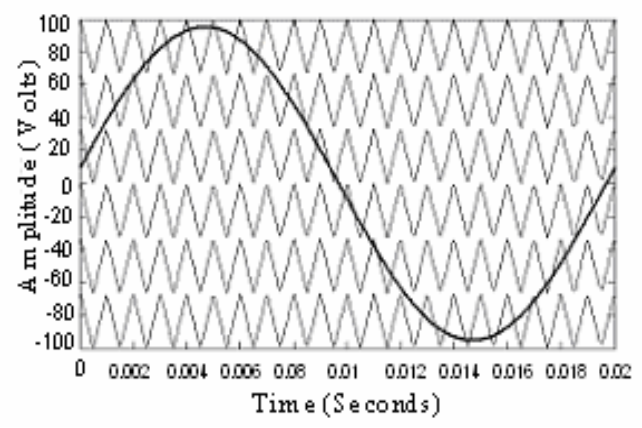

Fig. 3: Modulating and carrier waveforms for PDPWM.

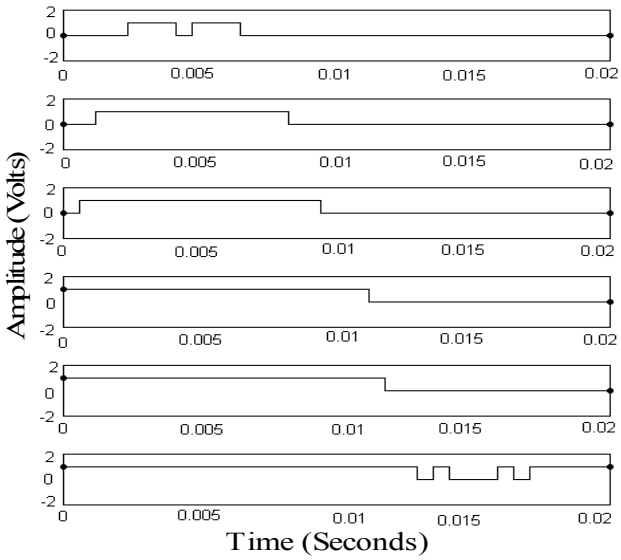

Fig. 4: Switching pattern for PDPWM

For a three-phase system, the value of frequency modulation index (m_f) should be multiples of three and if m_f is odd, the PD-method generates the lowest Total Harmonic Distortion (THD) value. The value of amplitude modulation index (m_a) is 0.95 and the frequency modulation index (m_f) is 21.

IV. Characteristics of a PEM Fuel Cell

The proton exchange membrane fuel cell (PEMFC) has been considered as a promising kind of fuel cell during the last 10 years because of its low working temperature, compactness, and easy and safe operational modes. The proton exchange membrane (PEM) fuel cell is very simple and uses a polymer (membrane) as the solid electrolyte and a platinum catalyst. The hydrogen from a pressurized cylinder enters the anode of the fuel cell and the oxygen (from air) enters the cathode. Protons and electrons are separated from hydrogen on the anode side. In a basic PEM cell, the protons are transported to the cathode side through the polymer and the electrons are conducted through the load outside the electrode. A fuel cell stack is composed of several fuel cells connected in series separated by bipolar plates and provides fairly large power at higher voltage and current levels.

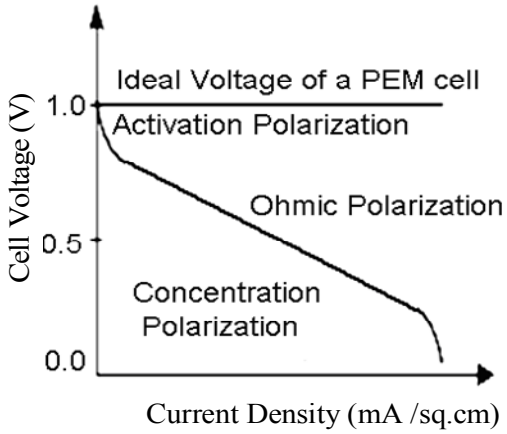

Fig. 5: Ideal VI characteristics of a single PEM fuel cell.

The electrical characteristics of the fuel cell output can be represented by current density versus voltage curve as shown in Fig. 5. The voltage at lower current density drops significantly at higher load current and maximum power occurs in theohmic region. Hence, ohmic region is used as a voltage window for the power conditioner unit input. Since the output voltage generated by each fuel cell is relatively low at full output current, they are stacked in series to produce the required voltage level. In this work a fuel cell unit with an output voltage of 40V is taken and the simulated polarization curve is shown in Fig. 6. And a high efficiency power conversion system is required for better operation. The power conditioning circuits for the fuel cell are inverters and dc/dc converters. In almost every application, ac power is required demanding the utilization of an inverter in the power conditioning system [7].

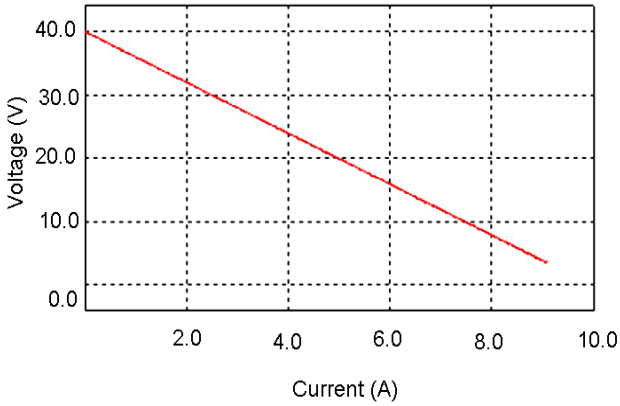

Fig. 6: Polarization curve of a 1kW PEM fuel cell.

And the literature shows multiple types of inverter designs. Also, if more power is required than what is available from the standard size fuel cell, and then modules need to be aggregated. There is more than one approach to aggregate numerous fuel cell modules for high voltage applications. One such approach is the multilevel architecture [8]. In this paper, a hybrid cascaded H-bridge multilevel inverter is proposed for the fuel cell power conditioning system as it not only requires a single dc source in each phase leg but also highly reliable and efficient.

V. Simulation Results

The simulation results for PDPWM based hybrid multilevel inverter for fuel cell power conditioning systems is shown in Fig. 7.

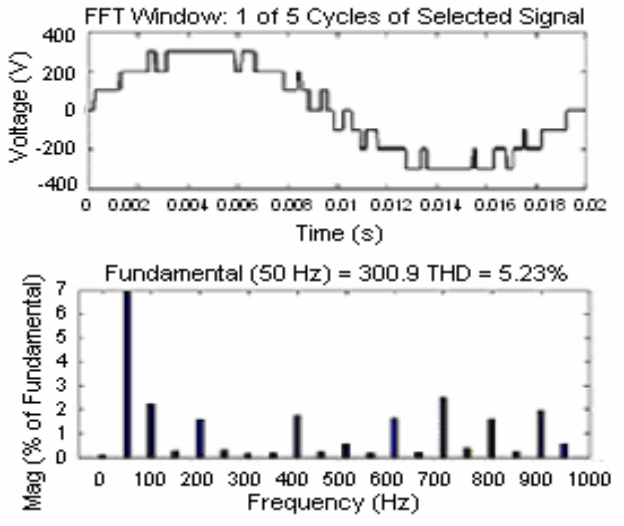

Fig. 7: Simulated output and FFT for PDPWM.

The work presents different pulse width modulation (PWM) control techniques for the hybrid seven-level cascaded multilevel inverter. The investigation is made in terms of Total Harmonic Distortion (THD) and switching frequency [9]. The Fig. 8. gives the harmonic spectra for the multicarrier pwm techniques. It gives a clear picture of the gap between the fundamental and the first significant harmonics for the various multicarrier pwm techniques. While using phase disposition for higher level systems, it is noted that the significant harmonics are locked to the carrier frequency and the gap between the fundamental and the first significant harmonics is decreased even though the amplitude of each harmonic around the carrier frequency is reduced. So, PDPWM seems to be favourable among the disposition techniques.

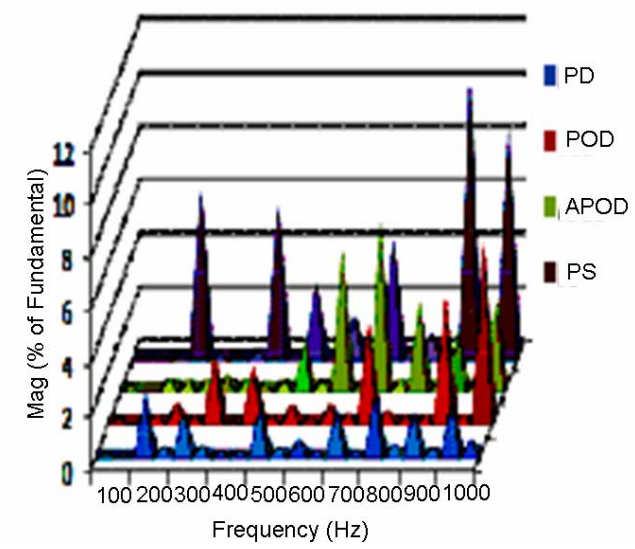

Fig. 8: Spectra for the various multicarrier PWM methods for ma =0. 95

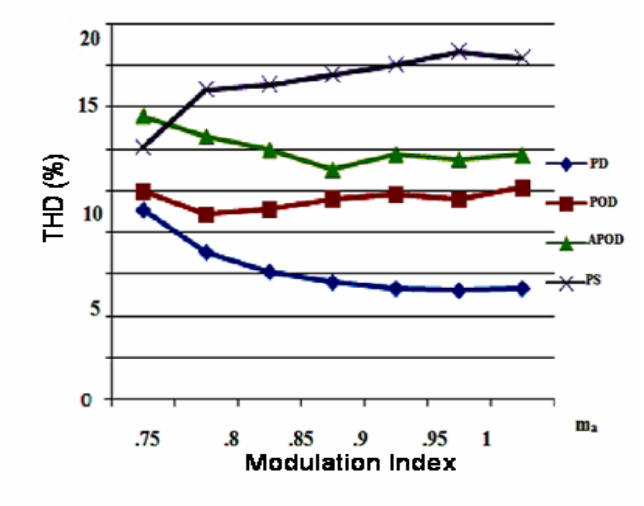

Fig. 9: THD for different multicarrier PWM methods

Fig.9.shows the line voltage THD for the hybrid multilevel inverter based on PD, APOD, POD and PS methods. From the results, it is found that for different amplitude modulation index (m_a) ranging from 0.7 to 1, the PD scheme achieves the lowest line voltage THD compared to other multicarrier PWM techniques. This is due to the fact that the PD method places significant harmonic energy into a carrier component for each phase leg, and relies on common mode cancellation between the inverter phase legs to eliminate this carrier energy from the line-to-line output voltage [10]. Consequently, the harmonic sidebands (which are not fully cancelled between the phases) have less energy. Also, from the simulation study conducted, many distinct features of hybrid MLI using PD scheme for the line voltage can be identified. The line voltage is able to synthesize more levels compared to phase voltage. Besides that, the line voltage yields better spectral performance, hence reducing the need for an output filter. Also, at high modulation index, the PDPWM technique introduces the lowest line voltage THD. PD method shows the lowest THD of about 5.23%. with f_c=1050 *kHz* and m_a= 0.95 as shown in Fig. 9.Hence PDPWM is employed for the hybrid cascade multilevel inverter.

VI. Experimental Results

To experimentally validate the proposed hybrid cascaded H-bridge multilevel inverter as shown in Fig. 1 for the fuel cell power conditioning system [11], a prototype seven - level inverter has been built using IRF450 Power MOSFETS as the switching devices. Only one dc source (fuel cell) was used for the hybrid cascaded MLI and the other source being capacitor (4700uF/100V -2nos in parallel) to generate seven levels. The gating signals were generated using FPGA processor based on phase disposition PWM techniques and the output power level of the inverter is 850W .From the Fig. 13. It is observed that the second level is constant at 20V and it is because of the main dc source. The first and third level requires capacitor voltage where the capacitor voltage is maintained at 10V. The corresponding FFT plot is also shown in Fig. 12. The gating pulses are shown below:

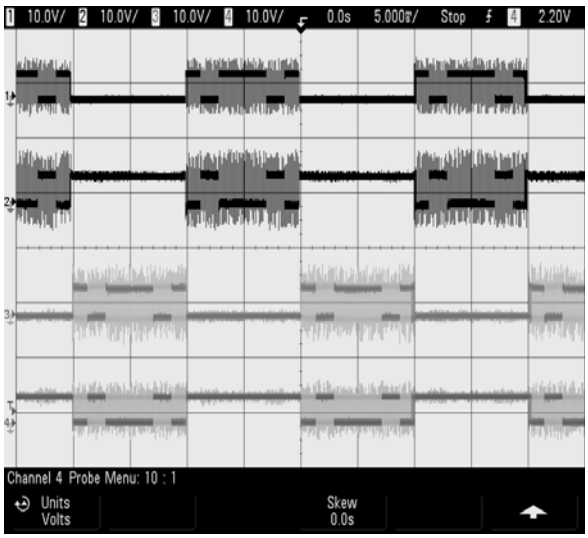

Fig. 10: Pulse pattern for the first bridge

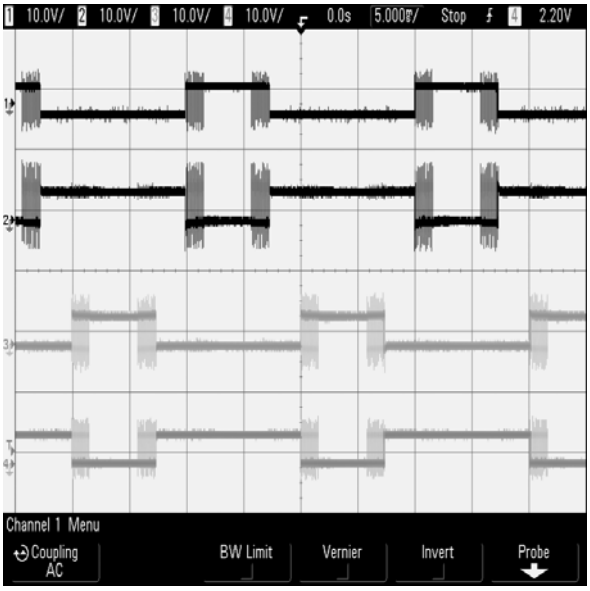

Fig. 11: Pulse pattern for the second bridge.

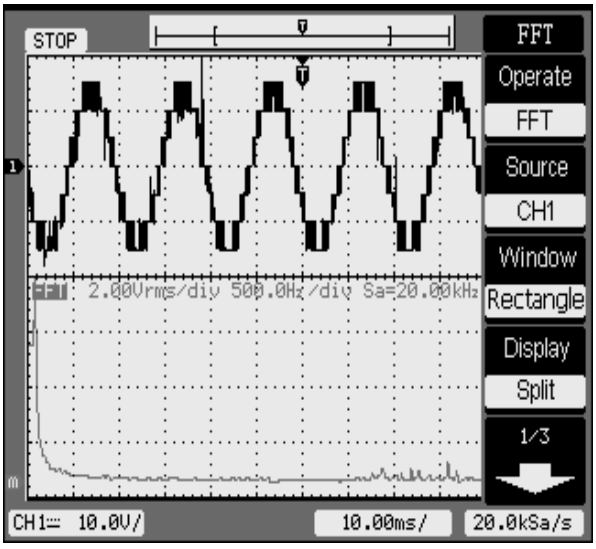

Fig. 12: Experimental output waveform and FFT for the hybrid seven–level inverter.

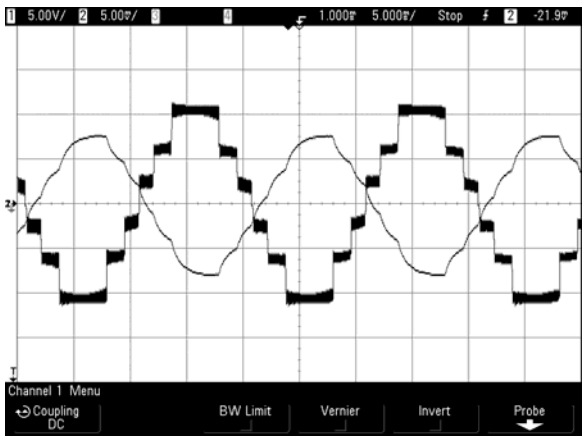

Fig. 13: Experimental equal 7-level output voltage and current waveform for the hybrid inverter with R=50Ω and L=36mH.

VII. Conclusion

In this paper, a hybrid seven level cascaded inverter have been investigated for fuel cell power conditioning system. A single dc power source and two H-bridges for each phase have been used as a good tradeoff between performance and cost. PDPWM technique is recommended as it gives least THD of about 5.23% at a modulation index of 0.95 and carrier frequency of 1050 kHz. This technique of modulation is better when compared with the APOD and PODS ones, as the PD scheme has advantages in three-phase applications due to the cancellation of the main carrier component between phase legs when the line voltages are formed [12]. At high modulation index, the PDPWM technique introduces the lowest line voltage THD. The results of simulation have been verified by experimentation. The proposed hybrid multi level inverter topology is suited for fuel cell electric vehicles motor for drive applications. With this PWM technique of hybrid MLI, it is possible to construct high power drives with high output voltage and low THD.

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